INTEGRATED DIRECT RF SAMPLING FRONT-END FOR VHF AVIONICS SYSTEMS

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Abstract

For a market sector where size, weight, power and cost (SWaP-C) optimization is crucial, specifically with the proliferation of unmanned aerial systems, this paper proposes the minimization of SWaP-C requirements through a Direct RF Sampling (DRFS) approach. This work focuses on the integration of avionics systems operating at the VHF band, i.e. VOR, ILS (LOC and GS) and aeronautical communications (voice, ACARS, VDL, etc.). The scope of this work is to present a feasibility study of the proposed integrated avionics. Several factors must be taken into account: First, the selection of a best sampling frequency is a key point in the design of the system. Two approaches to sampling frequency selection are considered: 1) static, whose aim is to digitize and lock the frequency bands fully; and 2) dynamic, where only the occupied channels are sampled without aliasing. The second important factor to be considered in addition to sampling frequency refers to the maximum dynamic range of the system. The dynamic range of the Analog to Digital Converter (ADC) has to be large enough to receive without distortion the most and the least powerful signals at the antenna. Finally, this work studies the digital down-converter (DDC) architecture to be hardware implemented in a Field Programmable Gate Array (FPGA), and quantitatively analyzes the resources required for its implementation.

Introduction

The minimization of equipment's SWaP-C requirements is a major objective in avionics systems design, utilizing optimally expensive cockpit real estate in modern commercial air carriers. Software Defined Radios (SDRs) represent a step beyond just to minimize all of these requirements. SDRs pave the possibilities of deep integration (i.e. ultra-tight) of almost all signal processing in software, leaving aside the problems related to hardware, thus significantly decreasing the cockpit real estate and weight of required equipment and redundant interconnecting hardware. SDRs perform at least as well as the old equipment and reduce the development, deployment and maintenance costs considerably; industry is pushing for technologies that have low life cycle costs of products. Moreover, a single SDR piece of equipment can be programmed to perform various functions or parallel avionics applications using common hardware.

This paper proposes the minimization of SWaP-C requirements through a DRFS approach. The minimization is achieved in two ways. On the one hand, by placing the ADC next to the antenna, the RF analog mixing section of the receiver is no longer needed. Subsequent filtering and down-conversion steps are carried out in the digital domain and implemented in a FPGA. The FPGA is also responsible for decimating the signal to a more tractable sampling frequency. On the second hand, the proposed DRFS approach allows sampling not only of the RF signal, but the entire frequency bands of interest. Thus, several systems share the same hardware as the signal separation is performed in the digital domain. This work focuses on the integration of avionics systems operating at the VHF band, i.e. VOR, ILS (LOC and GS) and aeronautical communications (voice, ACARS, VDL, etc.). Other systems operating in different VHF bands, such as VHF marker beacons (at 75 MHz), are not considered in this work, but can be included in future designs. Future papers from this research project will discuss DRFS technique extended to L and Ku bands of interest for satellite and avionics markets.

Commercial SDR platform manufactured by Nutaq, the PicoDigitizer, has been selected as the targeted platform for design and implementation of our preliminary proof-of-concept for the *intelligent avionics receiver*. With this platform in mind, this work presents a feasibility study for the proposed integrated avionics. Several factors must be taken into account: First, the selection of the sampling frequency is a key point in the design of the system. From the digital implementation point of view, the smaller the sampling frequency the better, as the

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signal processing resource requirements at the FPGA level increase with sampling frequency. However, using a sampling frequency that is too low will make the spectral bands of the various systems overlap at the output of the ADC. Two approaches to sampling frequency selection are considered: static and dynamic. In the static approach, the sampling frequency is selected in the design of the system, thus avoiding the overlap of various frequency bands in any condition. In the dynamic approach, the sampling frequency is selected while operating the system, as a function of the carrier frequency and bandwidth of the signals to be received. This second approach allows a better optimization of the digital resources required, but also produces an interruption of operation while the sampling frequency is reconfigured.

The second important factor to be considered refers to the maximum dynamic range of the system. The dynamic range of the ADC has to be large enough to receive without distortion the most and the least powerful signals at the antenna. Otherwise, additional hardware would be required to harmonize the power levels of each system. For instance, the signals with most power are those transmitted by the aircraft itself. The dynamic range of the incoming signals can be reduced by increasing the isolation between the transmitter and the receiver, so that the signal power received from the airborne transmitter becomes less than the maximum signal power expected from the ground. Note that the use of Automatic Gain Control (AGC) circuits in the receiver path can relax the dynamic range requirements of the ADC in many situations, but it cannot decrease the requirements for the worst case.

The paper ends with an initial estimate of the resources required in an FPGA in order to implement the integrated front-end design. The PicoDigitizer includes a Virtex-6 FPGA, which interfaces with a dual channel 250 MSPS ADC and dual channel 1 GSPS DAC. Finally the front-end architecture is described and an initial design for both, the static and dynamic approaches, are provided. The results demonstrate the feasibility of this front-end design implemented into the target SDR platform.

DRFS Approach

The DRFS approach proposed in this work is sketched out in Figure 1. In this approach, the RF signal at the antenna is digitized by an ADC using bandpass sampling (BPS). This technique employs a sampling frequency much smaller than required by Nyquist sampling theorem (twice the highest frequency). Consequently, the computational burden demanded from the FPGA is much less thus providing current hardware technologies for product implementation. For the systems considered, the sampling frequency can be decreased by a factor of several thousands. A complete analysis shall be provided in the following sections.

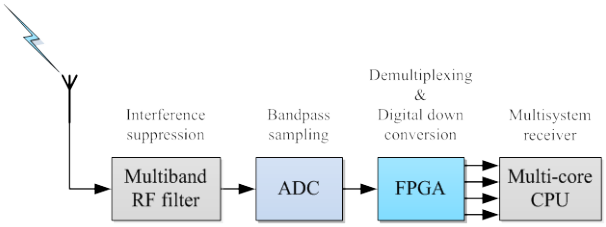


Figure 1. DRFS Mechanized Integrated Receiver

BPS mandates an additional complexity in the design of the RF anti-aliasing filter (AAF). Conventionally, AAF is a low pass filter which eliminates impinging signals at frequencies higher than the Nyquist rate. Through BPS, ideally the signals or spectral bands of interest cover the entire digital spectrum. Therefore, any interfering signal must be mitigated prior to entering the ADC. Figure 2 shows the spectrum allocation of the considered systems. It can be seen that there are two bands of interest: 108-137 MHz and 328.6-335.4 MHz. Thus, the required RF AAF is a multiband filter; as opposed to the low pass filter traditionally required (dynamic range issues shall be considered in detail in the next section).

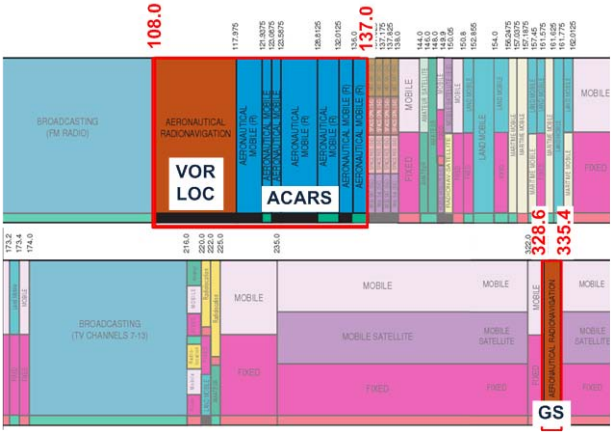


Figure 2. Spectrum Allocation: VHF Avionics Systems

The output of the ADC consists of several signals of interest located at different frequency channels. These frequency channels need to be demultiplexed, down-converted and downsampled before being transmitted to the CPU (a CPU can also be a software instantiation within the FPGA device). All these tasks are performed by an FPGA and represent the main focus of this paper. From the FPGA, a CPU receives a single low-rate data stream per channel, which can be processed simultaneously in a multi-core processor. As a result, the proposed DRFS system uses common core hardware to process signals at different frequency bands, from various avionics systems.

In the following sections, the most relevant requirements and design parameters are analyzed: First, the required amplification gain and dynamic range of the system is considered. A crucial requirement of the system is that the Spurious Free Dynamic Range (SFDR) of the ADC must be greater than the input dynamic range. Second, the selection of the most suitable sampling frequency is the main problem of the BPS technique. Final sections go a step further in the optimization of the sampling frequency by using a dynamic approach in which the channels being received change over time, or by reducing the channel guard bands.

Dynamic Range Analysis

In this section we determine the required dynamic range for the ADC. Assuming if the most powerful signal at the input of the ADC has been successfully brought to full scale, then the ADC's dynamic range can be used to get an estimate of the system sensitivity. From the sensitivity, an estimate of the maximum range can be obtained. The rationale employed in this section is to use maximum input power and range to determine the dynamic range of the ADC.

Table I indicates the required sensitivity for VOR, LOC, and GS and the equivalent field strength [1-3]. For reference, it also includes the maximum input power at which the receiver is required to satisfy the standards. For communications systems, reference values have been obtained from commercial equipment [4].

Table I. Sensitivity & Range Requirements

System	Sensitivity	Min. Field Strength	Max. Input Power Requirement
VOR	-93 dBm	-120 dBW/m^2	-27 dBm
LOC	-87 dBm	-114 dBW/m^2	-33 dBm
GS	-77 dBm	-95 dBW/m^2	-33 dBm
System	**Sensitivity**	**Criterion**	
ACARS	-102 dBm	(> 99% of messages)	
VDL	-98 dBm	BER < 10^{-3}	
Voice	-105 dBm	SINAD < 12 dB	

In order to avoid compromising on receiver's sensitivity, the noise and spurious signals introduced by the ADC must be low enough. The ADC available in Nutaq's PicoDigitizer is Texas Instrument's ADS62P49. The minimum SFDR of this chip for the frequency bands of interest is about -82 dBFS (dB relative to full scale) [5]. The ADC's noise power for 50-KHz channels is even less than -100 dBFS. Assuming worst case scenario, in order to achieve the sensitivity listed in Table I for voice communications, the highest spurious level at the ADC's output should correspond to less than -117 dBm. When this level is matched to the SFDR, -82 dBFS, the ADC's noise power becomes at least 10 dB below thermal noise floor [5].

In addition, ADC's full scale results in -35 dBm. This level is not enough to respect the maximum input power (see Table I) required by RTCA standards [4-6]. Indeed, it is 10 dB below VOR requirements, considering a clearance of 2 dB. Nevertheless, compliance with standards can be satisfied by selecting ADC's with a higher SFDR, such as the ADC16DV160, with 95 dBFS [6], or the LTC2145-14, with 90 dBFS [7].

But the more challenging requirements are those related to interfering signals and, by extension, integrity, availability and continuity. In a pessimistic scenario, the avionics systems will not operate under specifications anytime the input power exceeds the full scale equivalent power. With the DRFS

approach, the LOC system, for example, can be inoperative due to an excessive level of an incoming GS signal. This maximum input power can be converted into minimum range to ground facility through:

$$20\log_{10}(r_{min}) = P_{EIRP} + G_R - P_{FS} - 20\log_{10}(f) - 32.45 \qquad (1)$$

where r_{min} is the minimum range in Km, P_{EIRP} is the ground facility's Equivalent Isotropically Radiated Power (EIRP), G_R is the combined gain of the receiver's antenna and cabling losses up to the certified avionics equipment, P_{FS} is the full scale equivalent power, and f is the RF frequency in MHz. This minimum range is a conservative estimate since only free-space path loss is considered in (1).

Table II shows typical EIRP for different ground facilities [8], along with the minimum field strength required at the maximum coverage range that leaded to these values. When applicable, long range (or "en-route") ground facilities have been considered. For communications systems, 200W EIRP will be used as well as for the VOR system.

Table II. Typical Long Range Ground Facilities' EIRP

System	Typ. EIRP (Long Range)	Min. Field Strength Requirement	Max. Range
VOR	200 W	-107 dBW/m^2	200 NM
LOC	25 W	-114 dBW/m^2	25 NM
GS	10 W	-94 dBW/m^2	10 NM

Figure 3 plots the minimum range beyond which the ADC is saturated. The full scale equivalent power is -22 dBm. Considering $G_R = 0$ dB as common, the results show that the integrated front-end can become inoperative for distances shorter than 450 m to a LOC ground facility, or 1.2 Km to a long-range VOR/COMM. ground facility. Further investigation is required to determine the severity of the problem in real locations.

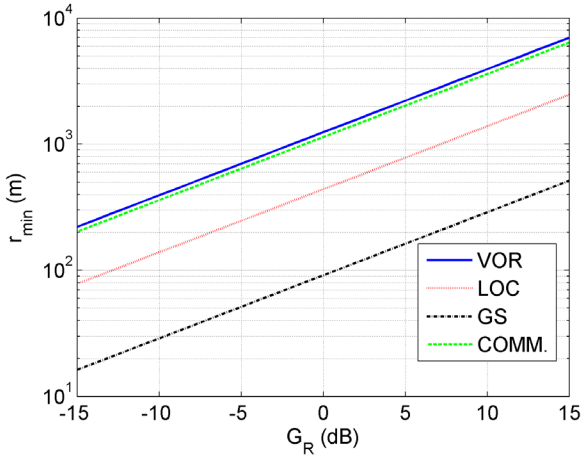


Figure 3. Minimum Range vs. Receiver's Antenna Plus Cabling Gain at 95 dBFS SFDR

A priori, two approaches can be followed in order to overcome this problem: using higher SFDR ADCs, or incorporating an Automatic Gain Control (AGC) circuit prior to the ADC. Increasing the SFDR is the ideal approach because sensitivity is not affected. However, current ADC technology does not offer this possibility as regards the required sampling rate, which is studied in the next section. As a result, the only realistic alternative consists in incorporating an AGC circuit prior to the ADC, even at the cost of a possible loss of sensitivity. Figure 4 represents the maximum sensitivity loss as a function of the distance between the ground facility and the avionics system. Taking into account these curves and normal flight operations, the sensitivity is not expected to degrade more than 10 dB.

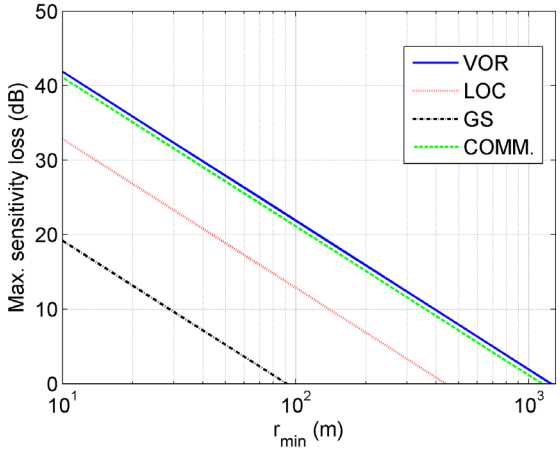


Figure 4. Maximum Sensitivity Loss vs. Minimum Range at 95 dBFS SFDR, and $G_R = 0$ dB

Sampling Frequency Selection

After defining the required dynamic range, the next step is to decide the sampling frequency for the bandpass sampling. As most suitable one, we choose the minimum rate that guarantees no overlap between different channels. Two different approaches are used depending on knowledge about the spectrum occupancy. The first approach uses no knowledge and therefore all the channels must be separable after digitization. The second approach is based on a perfect knowledge of what channels are vacant, and optimizes the sampling rate by allowing the aliases of vacant channels to overlap the non-vacant ones'.

Let us consider now the first approach. Since no overlap is allowed between channels, is twice the sum of bandwidths of all the spectral bands. From the frequency band limits shown in Figure 2, the minimum sampling frequency results in 71.6 MHz.

However, two additional constraints must be satisfied:

A Spectral Band Cannot Fold Up Over the Spectrum Limits

Formally, this means than both the lower and upper frequencies of the band (L and U, respectively) must fall in the same Nyquist zone :

$$N_k \equiv \left\lceil \frac{2L_k}{f_s} \right\rceil = \left\lceil \frac{2U_k}{f_s} \right\rceil, \ \forall\, k \qquad (2)$$

Where N_k is the Nyquist zone, f_s is the sampling frequency, $\lceil \cdot \rceil$ represents the ceil function, and the subscript "k" stands for the k-th spectral band.

This condition is evaluated for every spectral band. When this is not satisfied, the sampling frequency must be increased to f_s' :

$$f_s' = \frac{2U_k}{\left\lceil \frac{2L_k}{f_s} \right\rceil} \qquad (3)$$

Two Different Spectral Bands Cannot Overlap

Mathematically, this is equivalent to the following condition being true:

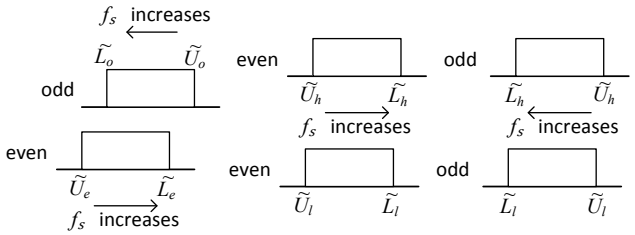
$$\left[\max\left(\tilde{L}_k, \tilde{U}_k\right) < min\left(\tilde{L}_j, \tilde{U}_j\right)\right] \vee \left[\min\left(\tilde{L}_k, \tilde{U}_k\right) > max\left(\tilde{L}_j, \tilde{U}_j\right)\right], \ \forall\, k \neq j \qquad (4)$$

Where the operator $\vee$ represents the "and" operator. The tilde superscript stands for digital frequency. Digital frequency can be obtained from the normalized frequency, $f_n = f/f_s$:

$$\tilde{f} = \begin{cases} |f_n - \lfloor f_n \rceil| \\ f_n - \lfloor f_n \rceil & \text{, for odd Nyquist zone} \\ \lfloor f_n \rceil - f_n & \text{, for even Nyquist zones} \end{cases} \qquad (5)$$

Where $\lfloor \cdot \rceil$ stands for the round (nearest integer) function.

The minimum and maximum functions in the above expression are needed for the case where the spectrum has been inverted (Nyquist zone is even), and thus $\tilde{L} > \tilde{U}$. If the condition in (4) is not satisfied, then the sampling frequency must be increased accordingly. Depending on the parity of the Nyquist zones of the involved spectral bands, three different cases must be taken into account. They are represented in Figure 5. The arrows indicate that digital frequencies corresponding to odd Nyquist zones decrease when the sampling frequency increases, but they increase with the sampling frequency for even Nyquist zones. The greater the Nyquist zone is, the greater the decrease/increase is.



(a)Odd/Even **(b)Even/Even** **(c)Odd/Odd**

Figure 5. Spectrum Overlap Cases

a) The overlapping spectral bands fall in odd and even spectral zones. This is the case in Figure 5 (a). From the drawing, the sampling frequency must be increased until the digital frequencies corresponding to the upper frequencies of each band are the same, $\tilde{U}_e = \tilde{U}_o$, where the subscript e and o stand for "even" and "odd", respectively. Thus, the sampling frequency becomes:

$$f_s' = \frac{U_o + U_e}{\left\lfloor \frac{U_e}{f_s} \right\rceil + \left\lfloor \frac{U_o}{f_s} \right\rceil} \qquad (6)$$

b) Both spectral bands fall in even Nyquist zones. This is the case represented in Figure 5 (b), where the subscripts h and l stand for "higher" and "lower" Nyquist zones, respectively. Since the digital frequency increases faster for the spectral band at the higher Nyquist zone, the overlap can be solved by increasing the sampling frequency such that $\tilde{U}_h = \tilde{L}_l$. This yields a new sampling frequency:

$$f_s' = \frac{L_l - U_h}{\left\lfloor \frac{L_l}{f_s} \right\rfloor - \left\lfloor \frac{U_h}{f_s} \right\rfloor} \quad (7)$$

c) Both spectral bands fall in odd Nyquist zones. Similar to the previous case, this one is represented in Figure 5 (c). The same rationale leads again to (7), which can be applied to this case as well.

However, the corrections in (5) and (6) are not valid if the sampling frequency increase implies a change of the Nyquist zone of the frequencies involved. The maximum sampling frequency so that these corrections are valid is:

$$f_{s_{max}} = \begin{cases} \min\left(\frac{2U_o}{\left\lfloor \frac{2U_o}{f_s} \right\rfloor - 1}, \frac{2U_e}{\left\lfloor \frac{2U_e}{f_s} \right\rfloor - 1}\right) & , \text{ case 2a)} \\ \min\left(\frac{2L_l}{\left\lfloor \frac{2L_l}{f_s} \right\rfloor - 1}, \frac{2U_h}{\left\lfloor \frac{2U_h}{f_s} \right\rfloor - 1}\right) & , \text{ case 2b) or 2c)} \end{cases} \quad (8)$$

When this bound is surpassed, the sampling frequency computed using the previous corrections is out of the range $f_s' \notin (f_s, f_{s_{max}})$, which can be used to impose the limit.

Algorithm 1 describes the procedure to obtain the minimum sampling frequency. By applying this algorithm to the case represented in Figure 2, a minimum sampling frequency of 137 MHz is obtained. This represents a decrease in the required sampling frequency by a factor of 5 compared to baseband sampling (670.8 MHz).

Algorithm 1: *Minimum Sampling Frequency*

0: Initialize the sampling frequency to twice the sum of bandwidths.

1: Check all the conditions in (2) and (4).

2: If any condition is not satisfied, then

a. Apply (6) or (7) accordingly, to increase the sampling frequency

b. If $f_s' \notin (f_s, f_{s_{max}})$: $f_s' = f_{s_{max}}$

c. Go back to step 1.

3: Otherwise, finish.

However, in practice it is necessary to consider the roll-off characteristics of the anti-aliasing multiband RF filter. If the center frequency of the VOR/LOC/ACARS and the GS frequency bands are maintained, but the bandwidths are gradually increased (and proportionally to the center frequency), the required sampling frequency also increases gradually until the bandwidth increase is 6.2287 % of the center frequency. This allows ample guard bands on each side: 3.8 MHz wide for the VOR/LOC/ACARS band, and 10.3 MHz wide for the GS band.

Static vs Dynamic FPGA Design

Despite decreasing the sampling by a factor of 5, the approach used in the previous section for determining the sampling frequency is highly inefficient. In practice, the number of VOR, ACARS and ILS ground facilities visible by an aircraft at a given time is quite reduced. Thus the occupancy of the spectral bands of interest is very low.

The second sampling frequency selection approach benefits from this fact and perfect knowledge of the channels in use at every moment. This knowledge can be inferred from the aircraft's position and the position of the various ground facilities. For example, a channel can be considered as used when the range to the corresponding ground facilities is less than a given value that guarantees the received signal power to be under the ADC's noise floor. Specific values for each facility can be determined using additional knowledge such as the transmitting power.

Using the same anti-aliasing multiband filter as before, the aliases of vacant channels are allowed to overlap with those from other channels, as they do not produce any interference on the other channel. The minimum sampling frequency required can be obtained using the same algorithm as before, but substituting the frequency limits of the whole band by the frequency limits of all the channels in use.

For example, Table III gathers VHF avionics channels in use around the Montreal's Pierre-Elliot-Trudeau International Airport area [9-11]. Using these values and Algorithm 1, the minimum required sampling frequency becomes 14.454 MHz approximately. This represents a decrease in sampling frequency by almost a factor of 10 compared to the static approach. The total improvement compared to baseband sampling is by a factor of 46.

Table III. Example: VHF Channels In Montreal Area

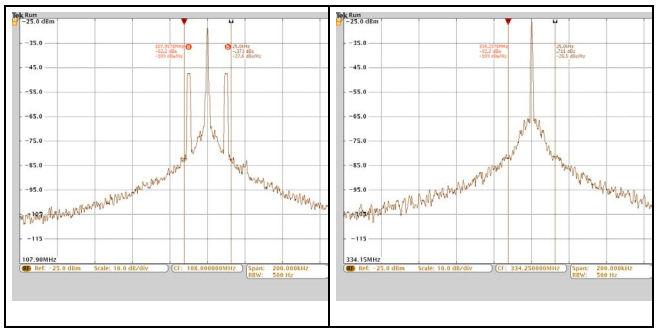
Center Frequency (MHz)	Channel Bandwidth (KHz)	Type	ID code
109.30000	50	LOC	IUL
332.00000	150	GS	
110.10000	50	LOC	IDO
334.40000	150	GS	
110.50000	50	LOC	IMQ/IOA
329.60000	150	GS	
111.90000	50	LOC	IZZ
331.10000	150	GS	
114.10000	50	VORTAC	KMSS
115.80000	50	VORTAC	CYJN
116.30000	50	VOR-DME	CYUL
116.70000	50	VOR-DME	CYMX
118.90000	25	Communications	CYUL
119.90000			
121.90000			
122.07500			
122.52500			
122.85000			
123.07500			
124.65000			
125.15000			
125.60000			
126.90000			
127.50000			
129.87500			
130.17500			
130.37500			
130.80000			
131.77500			
131.87500			
133.70000			
134.15000			

However, there is a drawback in this approach to select the sampling frequency: signal reception must be interrupted in order to reconfigure the channel selection. With the static approach, all the channels are available in the digital spectrum and adding a new channel can be as simple as writing a new carrier frequency value in an FPGA register. With the dynamic approach, there is no guarantee that the new channel is not overlapping with an already configured one. In case of overlap, the sampling frequency has to be recomputed, and the signal reception will be interrupted during the process of changing it.

Reducing the Guard Bands

Further sampling frequency optimization can be achieved by considering reduced guard bands for VOR/LOC and GS channels. The signal bandwidth for these systems is less than the channel separation leading to guard bands that can be seen as excessive as regards modern equipment [12]. For instance, the signal with the greatest bandwidth is VOR (around 20 KHz, see Figure 6.a), which suggests a channel bandwidth decrease up to 25 KHz. This channel bandwidth creates gaps of 25 KHz between the channels in the VOR/LOC spectral band; and those gaps can be occupied by GS channels.

Using this strategy, the sampling frequency can be decreased to 72.34 MHz using the static approach; or 7.875 MHz using the dynamic approach for the example in Table III. In both cases, the decrease in the sampling frequency is almost by a factor of 2.



(a) VOR **(b) GS**

Figure 6. Example of Signals Generated with Test Equipment Aeroflex's IFR-4000 (Vertical Markers Show Limits of Hypothetical 25-Khz Channels)

FPGA Implementation

The FPGA has three main functions to perform for each channel: 1) down-convert the signal to baseband; 2) filter out rest of the channels in the digital spectrum; and 3) decimate the signal to reduce CPU load and throughput required for the FPGA-CPU interface. Since the FPGA processes multiple channels in parallel, the channels' outputs are multiplexed into a single data stream that is sent to the CPU. For simplicity, all of the FPGA channels produce the same data rate, which in our example we have set to 50 KSPS (complex samples). Figure 7 graphically represents the block diagram of the signal processing carried out within the FPGA. Every reception channel can be tuned to a specific RF channel by writing the corresponding carrier frequency value (at the ADC output) into a writable register.

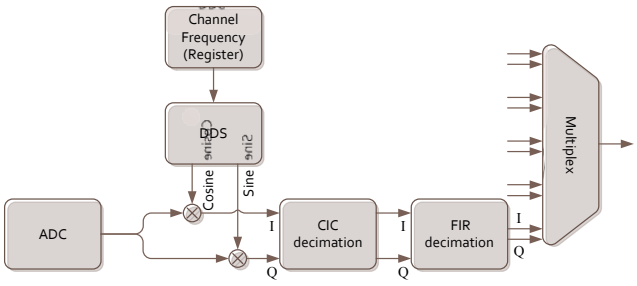


Figure 7. FPGA Architecture per Channel

The real signal digitized by the ADC is down-converted to baseband by multiplying it with a complex exponential generated by a DDS (Direct Digital Synthesizer). The frequency of this complex exponential is taken from one of the registries of the FPGA, which can be programmed externally, e.g. by the CPU. This allows selecting the received channel from the CPU while the receiver is running. Then, the signal is low-pass filtered and downsampled at the same time, but in two steps. First, a CIC (Cascaded Integrator-Comb) filter is used to reduce the high sampling rate of the ADC. Then, a second low-pass FIR filter equalizes the passband response of the CIC filter while performing further filtering and decimation.

The configuration parameters, for the static and dynamic case studies, of the elements composing the channel down-conversion chain are reflected in Table IV. Simulation results show that the carrier-to-noise ratio is degraded about 5 dB within the passband when this configuration is used.

Table IV. Filter Design Parameters

Item	Parameter	Static	Dynamic
ADC	Sampling rate	173 MSPS	14.5 MSPS
	Output word length	14 bits	
DDS	SFDR	96 dB	
	Resolution	25 KHz	
	Output word length	16 bits	
CIC	Decimation	548	58
	Number of stages	5	
	Differential delay	2	
	Output sampling rate	250 KSPS	
	Input word length	16 bits	
	Output word length	67 bits	51 bits
FIR	Cutoff frequency	12.5 KHz	
	Passband ripple	0.1 dB	
	Stopband attenuation	60 dB	
	Decimation	5	
	Length (number of taps)	88	
	Output sampling rate	50 KSPS	
	Decimation	5	
	Output word length (bits)	32	

Implementation Results

The above design has been simulated in software using Xilinx's System Generator. This platform has been selected because it will facilitate the future implementation of the system into the targeted PicoDigitizer through Nutaq's Model-Based Design Kit (MBDK).

In order to test the dynamic range of the system, three different RF signals are combined at the ADC input. The first one is a weak signal centered around 108 MHz, composed of three tones whose respective amplitudes are 90 dB below the full-scale value of the simulated ADC. The frequencies of the two adjacent tones correspond to ±12.5 KHz around the center frequency of 29 MHz, i.e. the channel limits. The second signal consists of a powerful tone at the center frequency of the contiguous channel (108.25 MHz), while the third and last signal is also a powerful tone at a frequency that is located at the first side lobe of the CIC filter (+108.5 KHz) after the down-conversion step. When the receiver is tuned to receive the first signal (the weak one), there is an alias of this tone at 8.5 KHz. This last tone will overlap with the first signal when both signals are generated with a power corresponding to 49% of the full-scale value.

Figure 8 represents the spectrum of the three signals as they appear at the output of the ADC using a sampling frequency of 137 MHz. The simulated ADC is ideal and uses 14 bits, and the SFDR is approximately 130 dBFS, as seen in Figure 8.

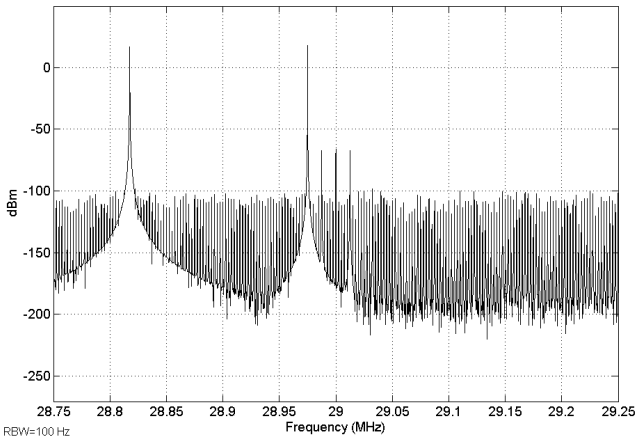


Figure 8. Spectrum at the Output of the ADC

Figures 9 to 11 show, respectively, the outputs of the channels corresponding to each of the three signals described above (Channel 1 for the first signal, and so on). Three main results can be extracted: First, the dynamic margin of 90 dB has been kept, and no spurious signals can be tolerated within the bandwidth of any channel. The peak at -25 KHz visible in Figure 9 corresponds to the tone in the adjacent channel, which has been attenuated by about 70 dB. The tone at 13.5 KHz in Figure 10 corresponds to the tone of the first signal located at the channel edge, and thus it has not been attenuated. Second, the DDS implementation has limited accuracy when generating tones that are not integer divisors of the system clock frequency, which was set to 137 MHz. This is why the baseband channel spectra appear slightly shifted in frequency. Consequently, special care should be taken on the selection of channel digitized bandwidth (given by the FIR filter) and the DDS frequency resolution. In our implementation, both have been set to 12.5 KHz. The third and final result is that the SFDR at the channel output has decreased by about 20 dB, to a maximum of 110 dBFS. This loss is the result of several truncations between the different elements in the receiver chain. In practice, this value must be greater than the ADC's SFDR, which is attained by our design.

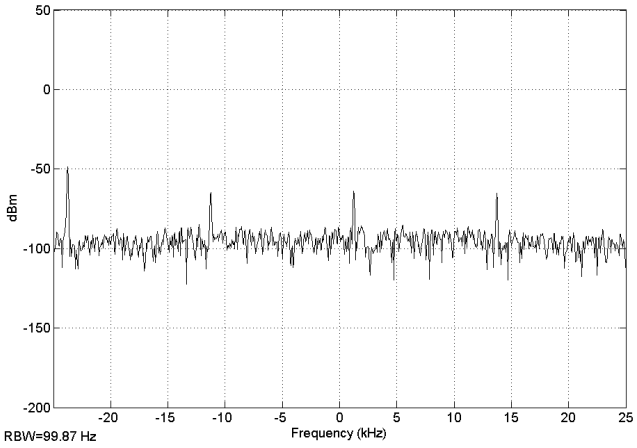


Figure 9. Spectrum at the Output of Channel 1

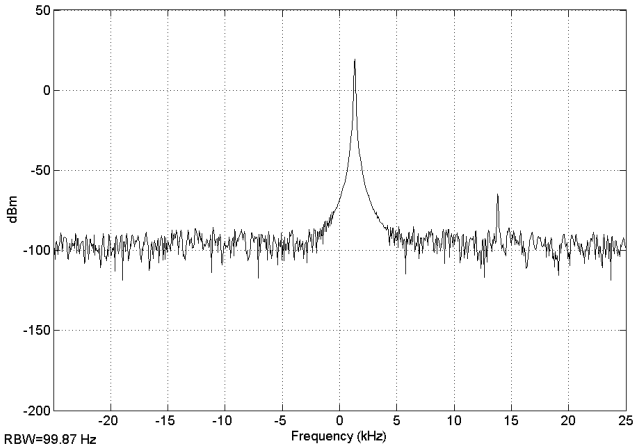


Figure 10. Spectrum at the Output of Channel 2

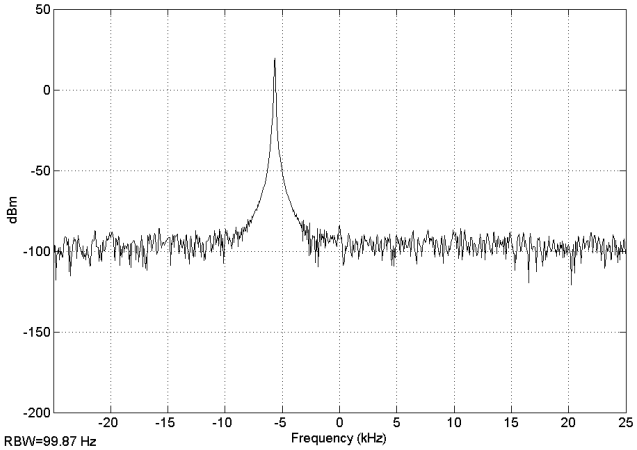


Figure 11. Spectrum at the Output of Channel 3

After the operational validation of the front-end it is also important to assess the FPGA resources required to implement the design. Table V summarizes the resource utilization report for the Virtex 6 FPGA resident in the PicoDigitizer. The optimization targets when generating a bitstream is minimize FPGA area. The table gathers the resources consumed by every element, by a single channel, and by 10 channels. It can be seen that the most used component are DSPs, with 28 per channel. However, if needed, the use of DSPs by the CIC filter can be drastically decreased at the cost of a higher use of logic. We observe that nothing in Table V indicates that our design is not implementable.

Table V. Resources Used

Item		Absolute	Relative
DDS & Mixers	Registers	356	0.1%
	LUTs	201	0.1%
	Slices	89	0.2%
	BRAMs	1	0.1%
	DSPs	2	0.1%
CIC	Registers	1,908	0.5%
	LUTs	810	0.4%
	Slices	439	0.9%
	BRAMs	0	0.0%
	DSPs	24	1.8%
FIR	Registers	461	0.1%
	LUTs	471	0.2%
	Slices	196	0.4%
	BRAMs	0	0.0%
	DSPs	2	0.1%
1 Channel Totals	**Registers**	**2,725**	**0.7%**
	LUTs	**1,482**	**0.8%**
	Slices	**724**	**1.5%**
	BRAMs	**1**	**0.1%**
	DSPs	**28**	**2.1%**
10 Channels Totals	**Registers**	**25,247**	**6.4%**
	LUTs	**12,983**	**6.6%**
	Slices	**6,605**	**13.4%**
	BRAMs	**10**	**1.4%**
	DSPs	**280**	**20.8%**

Finally, regarding the maximum number of channels allowed, this will depend on the resources consumed by the rest of the FPGA cores, such as those implementing the device interfaces. In addition, the number of channels is related to the total decimation factor, and thus, they should be taken into account when determining the other. The reason is that the interleaver (multiplex) at the back-end in Figure 7 requires to output samples at a rate that is an integer divisor of the system clock, which is set to an integer number of the sampling frequency, and often they are the same. As a result, the number of channels must be an integer divisor of half the total decimation factor. In our design, this implies than the valid number of channels go from 10 to directly 137. The problem can be solved by changing the total decimation factor according to the targeted number of channels. For example, 32 channels are possible by using a total decimation factor of 2752 (instead of 2740) which results in 49.78 KSPS per channel.

Conclusions

This work describes a feasible DRFS approach to integrated VHF front-end for avionics systems. The analysis of the sampling frequency and dynamic range requirements yields that ADC's currently available in the market can meet these requirements. Two different approaches were used to determine the minimum required sampling frequency depending on whether the empty channels are allowed to overlap with other channels or not. Allowing the overlap can result in decreases of the sampling frequency by a factor of 10, but it may affect other requirements such as availability or continuity.

Based on this analysis, we propose a design for the front-end. Preliminary performance results and FPGA resource consumption supporting the viability of the system are also provided. Future steps consist of implementing and testing the system both in-lab and in-flight.

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