Amplitude Demodulation based on Synchronized Sampling by a PLL Circuit

Zied Koubaa, Mohamed Ali
Polystim Neurotech Lab, EE Dept,
Polytechnique Montreal
Montréal, Canada
zied.koubaa@polymtl.ca

René Jr. Landry
LASSENA Lab., EE Dept,
École de technologie superieure
Montréal, Canada
ReneJr.Landry@estmtl.ca

Mohamad Sawan
Polystim Neurotech Lab, EE Dept,
Polytechnique Montreal
Montréal, Canada
mohamad.sawan@polymtl.ca

***Abstract*—In this paper, we present a new radio frequency receiver dedicated for avionic signals which can be used for distance measuring and air control traffic system. The designed system, based on the direct radio frequency sampling approach, uses a smart sampling to digitize and demodulate the received signal at the same time. The presented design is composed of a Phase-Locked Loop and a Delta-Sigma modulator and integrated in a 130 nm CMOS technology. Matlab simulations demonstrate the sensitivity of the system to the jitter and its effect on reliability. Using circuit simulation under Cadence environment, we have proved that our design achieved the expected demodulation performance with a low clock jitter.**

Keywords— DRFS, DME, TCAS, ADS-B, avionic applications, PLL, Delta-Sigma ADC, Amplitude demodulation, clock jitter.

I. INTRODUCTION

Radio Frequency (RF) front-end includes the whole circuit from the antenna to the digital processing module. The front-end contains two paths, one for the receiver and another for the transmitter. A lot of research continues to focus on the receiver path in order to enhance the received signal and convert the RF signal to baseband and digital data forms.

Different receiver architectures can be found in literature. The super-heterodyne was the most used receiver by designers. It is known for its good reliability and immunity to DC offset issues. However, in order to reduce the input frequency in the heterodyne receiver, intermediate down-conversion mixers followed by a filters are used. This method also uses at least an oscillator circuit and two mixers for the synchronization with the carrier signal. Therefore, super-heterodyne architecture is complex, hard to integrate in one chip, and requires many analog components which have a nonlinear response and large amount of power consumption [1].

On the other hand, the zero-IF receiver is less complex, so it is better to be used for integrated RF front-end solutions. In which the RF signal is converted to baseband frequency without the intermediate stage, which allows to reduce both the power consumption and the integration process, but it comes with drawbacks such as the flicker noise, DC offset and distortion [2]. Some designers prefer to use low-IF receiver in order to benefit from the advantages of both the zero-IF and the heterodyne methods. However, this architecture entails higher power consumption [3].

The three above-mentioned topologies have a considerable analog part of their system, which creates reliability, size and cost challenges. Direct RF Sampling (DRFS), which considered the most recent topology, allows maximal processing of the signal in the digital part by moving the ADC just after the LNA and the anti-aliasing filter [4]. Therefore, DRFS can be considered for avionic signals.

In this paper, we introduce a novel receiver design based on DRFS topology. The proposed receiver is designed to deal with Distance Measuring Equipment (DME), Traffic Collision Avoidance System (TCAS) and Automatic Dependent Surveillance-Broadcast (ADS-B), which used in aircraft for distance measuring and air control traffic system. Those signals are Amplitude-Shift Keying (ASK) or Amplitude Modulated (AM). The widest baseband frequency is 6 MHz and its carrier frequency is centered between 962 MHz to 1.2 GHz. By applying the Nyquist theory, the required ADC should sample at a minimum frequency of 2.4 GHz and at a higher frequency if a Delta-Sigma ADC (ΔΣ-ADC) is to be adopted. In latter case, we estimate that the sampling frequency should be 640 GHz for 10-bit accuracy, where the power consumption becomes higher and the design of a ΔΣ-ADC will be impossible. For these reasons, our objective is to propose a low-power consumption DRFS system with acceptable resolution.

The delta-sigma is the appropriate architecture to design a high resolution ADC in an integrated circuit. Typically, with this kind of signals, designers use a Bandpass ΔΣ Modulator (BP-ΔΣM) whose oversampling ratio is related to the large band of the spectrum and not to the maximum frequency. The integrator of BP-ΔΣM, however, needs an inductor and a capacitor components [5], which increases the chip area. In addition, the high frequency operation leads to high power consumption [6].

Bandpass sampling approach is another solution that can be used to process the modulated signals like ADS-B, DME and TCAS. The optimal sampling frequency in this approach is given by [7]. In frequency-domain, the sampling process consists of the repetition of the spectrum signal which is positioned in multiples of the sampling frequency. This method needs more processing after sampling to retrieve the useful data [8]. The converter in the Bandpass sampling solution can be a lowpass ΔΣ modulator (LP-ΔΣM).

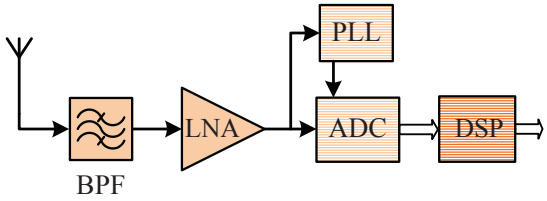

Fig. 1. Proposed structure of the data acquisition module.

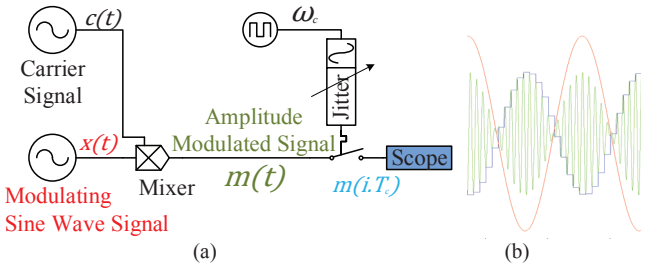

Fig. 2. (a) Simulated model in Simulink with indicated signal name, (b) Generated signals waveforms with corresponding colors.

To simplify the design and reduce the oversampling frequency, we proposed a new conversion method to demodulate the received signal (ASK or AM). The proposed architecture shown in Fig. 1 contains LP-ΔΣM and a Phase-Locked Loop (PLL). The PLL is used to generate a clock signal synchronized with the carrier signal. This clock signal is used to sample the received signal.

In section II, we present the proposed architecture, the role of each module, the simulation results and we explain the jitter effect in the sampling and the demodulation processes. Section III describes the PLL module. In section IV, the circuit-level implementation is described. The simulation results for the PLL are presented in section V. Conclusions are summarized in section VI.

II. Description Of The Proposed Architecture

A. Concept of the proposed architecture

We focus in this approach on the time-domain of the AM signal, where each peak of the modulated signal (x(t)) portrays the waveform of the modulating signal (m(t)):

$$x(t) = c(t).m(t) = A_x \sin(\omega_c t).m(t) \quad (1)$$

where c(t) is the carrier signal and A_x is a constant.

If we sample x(t) at each peak (t_i = i T_c), we obtain the modulating waveform sampled at the carrier frequency:

$$x(t_i) = A_x \sin(\omega_c t_i).m(t_i) = A\, m(t_i) \quad (2)$$

The two most important advantages of the proposed method are: (1) To provide a simple demodulation using a sampling process, (2) To sample the received signal at a frequency higher than the Nyquist frequency of the modulating signal; this over-sampling is used by the Delta-Sigma Modulator (ΔΣM) to increase the conversion resolution.

To avoid the distortion in the extracted m(t), the received signal should be sampled at each peak. So, the ADC clock signal should be synchronized with the carrier signal. Thereby, the architecture contains a PLL module to generate the needed clock (Fig. 1). Fig. 2 shows the used model in Matlab to validate the system functionality and to define its theoretical parameters.

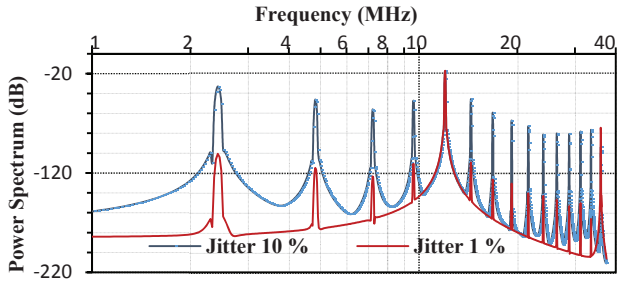

Fig. 3. Power spectrum of the output signal for a jitter of 1% and 10 %.

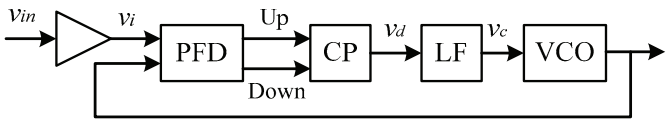

Fig. 4. Main building blocks of the PLL circuit.

B. Jitter effects in the proposed system

The clock signal is generated by PLL. So, jitter effects is considered in the A/D process. According to [4, 9], the effect of the clock jitter depends on its value and on the frequency of the input signal. Thus, the same jitter value has a larger impact on data conversion for higher-frequency signals.

In this work, we handle the jitter issues because it directly affects the demodulation process as well as the A/D conversion. Although the proposed system works like a sampling of the modulating signal (low frequency), the real input frequency is that of the modulated signal (high frequency). Therefore, the jitter's effect on the direct sampling is greater than that in the traditional methods.

To evaluate the jitter effect on the signal sampling, we chose two values of the jitter; 1% and 10 %. Fig. 3 shows the power spectrum of the output signal with the two selected values of jitter. Simulation results (Fig. 3) explain that the jitter adds harmonic components and their amplitudes increase with the jitter value. When the input is the modulated signal, the calculated Signal-to-Noise and Distortion Ratio (SNDR) for 1% jitter is decreased only by 2.5 dB, and it is decreased by 35 dB for 10% jitter. While the calculated SNDR for 10 % jitter is decreased only by 6 dB when the input is the modulating signal.

III. Synchronization Circuit: PLL

The performance of the demodulation depends primarily on the ability of the PLL to generate a synchronized signal with the carrier. As shown in Fig. 4, the PLL is composed of a Phase Frequency Detector (PFD), a Charge Pump (CP), a loop filter, and a Voltage-Controlled Oscillator (VCO) [2]. The PLL receives an amplitude modulated signal ($v_i(t) = V_i \sin[\omega_0 t + \Phi(t)]$) and the VCO generates a periodic signal ($v_0(t) = V_0 \cos[\omega_0 t + \widehat{\Phi}(t)]$) whose frequency is controlled by the input voltage (v_c). The output signal from the VCO is used as a reference for the PFD. In the steady state, the control signal (v_c) will be constant and the reference signal should be in phase and synchronized with the input signal.

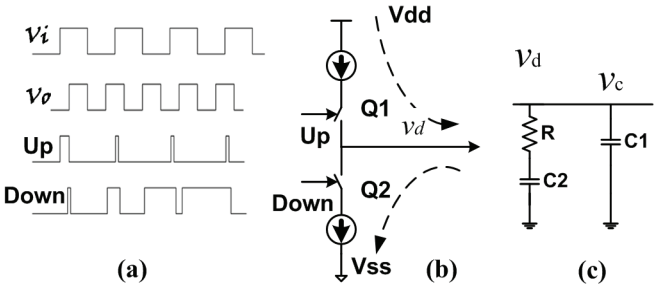

Fig. 5. (a) Input and output waveforms for the PFD, (b) Simple CP circuit (c) Second-order loop filter

The PFD is used to compare the input signal with the reference signal and it produces *Up* and *Down* signals. The logic state of each of the two signals depends on the frequency and the phase difference between v_i and v_0 as shown in Fig. 5(a). These two generated signals control the direction of the CP current (Fig. 5(b)). The loop filter shown in Fig. 5(c) is used to convert the CP current into voltage [10].

In the proposed architecture, the VCO generates the sampling clock whose phase variation is proportional to the v_c. Consequently, the origin of the jitter would be either the nonlinearity response of the VCO or the instability of v_c. Since the sampling process has to be done at the peak, the phase of generated clock should be shifted by $\pi/2$ with the carrier signal. Therefore, it is necessary to design a VCO with a low jitter and provides the required phase shift.

IV. Circuit Design

Given that the carrier frequency of the DME signals varies in the range of 975 MHz to 1.2 GHz, the PLL is designed to operate and generate the sampling clock at the same range. However, the maximum frequency of the modulating DME/ TCAS signal is 6 MHz and 2 MHz for the ADS-B, which means that the obtained output signal will be over-sampled.

A. Delta-Sigma Modulator

We design a high resolution integrated ADC using the ΔΣ architecture which is based on the oversampling technique to increase the SNDR of the baseband signal. In our design, the sampling clock, synchronized with the carrier signal by the PLL, attains a high oversampling rate (greater than the Nyquist rate).

Fig. 6(a) shows the simplified architecture of the ΔΣ-ADC; the ΔΣ-M (the analog part) is responsible for the input signal over-sampling. Therefore, the level of the quantification noise of the signal decreases as the sampling frequency increases. In addition, the quantification noise is shaped at high frequency by means of ΔΣ modulation process. The decimation filter (the digital part) reduces the high-frequency noise components in order to lower the sampling ratio to the Nyquist level, while maintaining a good resolution (high SNDR at the baseband of the signal).

There are two architectures for the ΔΣ-M; the continuous-time (CT-ΔΣ, Fig. 6(b)) and the switched-capacitor (SC-ΔΣ, Fig. 6(c)). The latter is suitable for our application due to the position of the sampler (the switch). The proposed method is based on sampling the waveform of the modulating signal by selecting specific instants of the modulated signal. However, the filter in the SC-ΔΣ (Fig. 6(c)) needs an operational

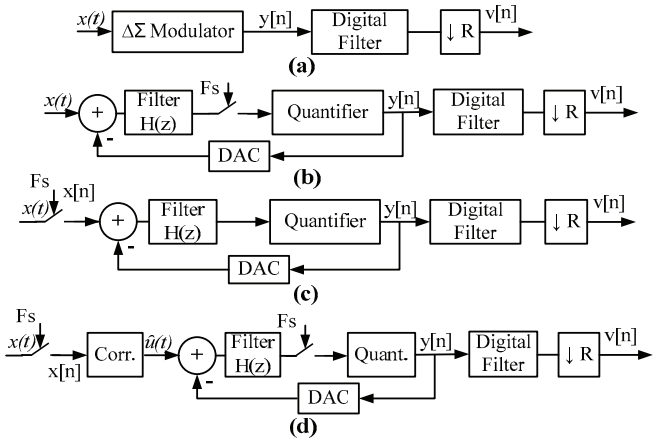

Fig. 6. Block diagrams of differnent ΔΣ-ADC topologies (a) Main ΔΣ-ADC (b) CT-ΔΣ-ADC, (c) SC-ΔΣ-ADC, (d) The Proposed ΔΣ-ADC.

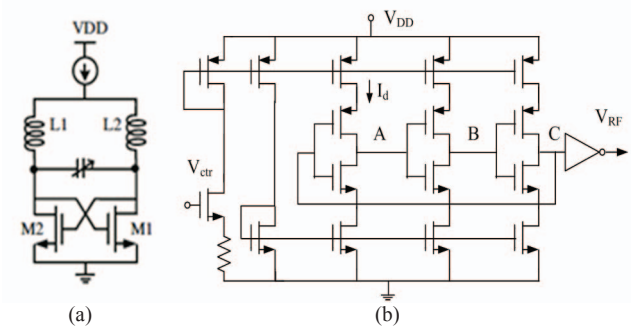

Fig. 7. (a) Schematic of the LC-VCO, (b) Schematic of the ring VCO

transconductance amplifier (OTA) with a bandwidth 5 times the sampling frequency (6 GHz). This disadvantage makes the ADC design more difficult. In the first architecture, the OTA bandwidth should be 2 GHz and its design is easier than that of the SC-ΔΣ. For this reason, the proposed ΔΣ-M design shown in Fig. 6(d) is based on CT-ΔΣ-M with an added sampler at the input followed by a correcting circuit.

B. Voltage Controlled Oscillator

The VCO determines the purity of the signal spectrum generated by the PLL. The most important characteristics of this circuit include the linearity, the frequency range, the phase noise, and the silicon area. There are two main VCO topologies; the LC-VCO and the ring VCO.

As shown in Fig. 7(a), LC-VCO is composed of a resonator and an amplifier. The resonator circuit is an LC-tank, whose resonant frequency (f_c) is controlled by the input voltage; the control voltage changes the capacitor value and consequently the oscillation frequency changes.

The ring architecture consists of an odd number of cascaded inverters (Fig. 7(b)). These inverters are connected like a ring, and the oscillation frequency is defined by the propagation delay of the signal inside the ring. So, the frequency value depends on the number of stages (N) and the rate of charge or discharge of the total capacitance seen at the output of each inverter (C_{tot}). The time of each charging and discharging is controlled by the polarization current of each stage (I_d). The running frequency is defined by:

$$f_c = {}^{I_d}/_{NC_{tot}Vdd} \quad (3)$$

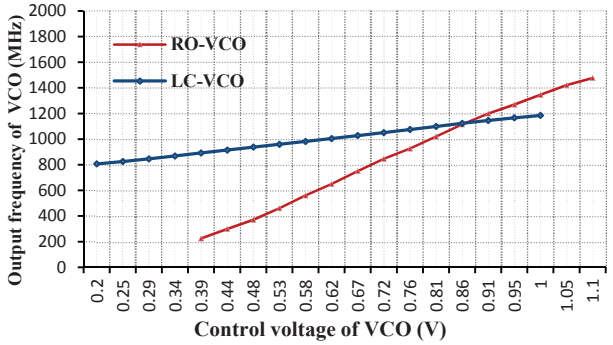

Fig. 8. Output frequency according to the control voltage variation

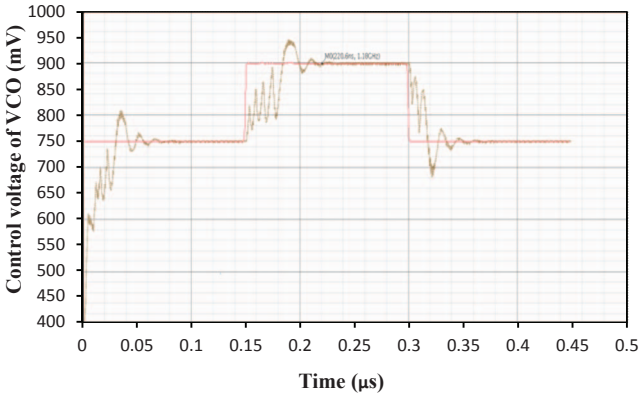

Fig. 9. The transient simulation for the PLL

By assuming equal delay in each inverter, the signal at point A in Fig. 7(b) is shifted by π/2 with the output signal (V_{RF}). Therefore, this signal is used as a sampling clock for the ADC.

V. Simulation Results

The simulation results of the two VCO designs are presented in Fig. 8, which depicts the output frequency of the two VCOs versus the input control voltage. It is clear that the ring VCO provides a wider tuning range than LC-VCO and its linearity is improved by means of using a resistor as shown in Fig. 7(b). The ring VCO exhibits a phase noise of -84.2dBc/Hz@1MHz offset from 1GHz frequency and it consumes 112.51µW at 1 GHz output frequency. The phase noise of the LC-VCO is -108.2dBc/Hz@1MHz and it consumes 627.84µW when it operates at 1GHz.

Despite it has a lower phase noise, LC-VCO consumes more power and silicon area compared to ring VCO. In addition, ring VCO provides a sampling signal which is shifted by π/2 with the output signal. So, ring VCO is considered in the PLL design. The PLL response is evaluated for the maximum frequency change (from 800MHz to 1.2GHz). Fig. 9 shows the transient simulation for the PLL. It is clearly seen in the figure that the input frequency is changed at 150ns from 800MHz to 1.2GHz and the PLL successfully tracked this change in less than 70 ns.

The performance of the proposed design is summarized and compared to other DRFS receivers from the recent literature in Table I. In this work, the sampling frequency is the lowest which allows providing higher resolution.

TABLE I. DRFS Receiver Performance Comparison

Parameter	[5]	[11]	This work
Topology	DRFS	DRFS	DRFS
ADC Architecture	BP-ΔΣM	BP-ΔΣM	LB-ΔΣM
Input Freq. (MHz)	800 -1924	900	975 - 1200
Clock Freq. (GHz)	1.6 - 3.2	3.6	0.975 – 1.2
Power consumption (mW)	30 + 11 (ADC + PLL)	15 (ADC)	22 + 0.387 (ADC +PLL)
Resolution (bits)	8	8	10
Process	0.13 µm CMOS	0.13 µm CMOS	0.13 µm CMOS

VI. Conclusion

This paper presents the design of a DRFS receiver for avionic signals. The proposed method based on a smart sampling process for digitizing and amplitude demodulating the received signal. The theoretical explanation of the proposed solution was presented and its sensitivity to the jitter was analyzed. The circuit implementation of the PLL is introduced. A low-phase-noise PLL was successfully designed and simulated in IBM 130 nm CMOS technology. Moreover, the proposed topology can be further extended to other demodulation applications; FM, QAM, etc.

Acknowledgment

The authors acknowledge the financial support from NSERC, CRIAQ, MITACS, Bombardier, MDA and Marinvent Corporation, and the design tools from CMC Microsystems. They would like also to express their gratitude to all of the AVIO505 project members for their valuable advice to improve this manuscript.

References

[1] H. Chae et al., "A 12 mW Low Power Continuous-Time Bandpass ΔΣ Modulator With 58 dB SNDR and 24 MHz Bandwidth at 200 MHz IF," IEEE J. Solid-State Circuits, vol. 49, pp. 405-415, 2012.

[2] H. Darabi et al., "Highly Integrated and Tunable RF Front Ends for Reconfigurable Multiband Transceivers: A Tutorial," IEEE Trans. Circuits Sys. I, Reg. Papers, vol. 58, pp. 2038-2050, 2011.

[3] M. Kitsunezuka et al., "A low-IF/zero-IF reconfigurable analog baseband IC with an I/Q imbalance cancellation scheme," IEEE J. Solid-State Circuits, vol. 46, pp. 572-582, 2011.

[4] G. Lamontagne and A. B. Kouki, "Direct RF Sampling GNSS Receiver Design and Jitter Analysis," 2012.

[5] Gupta, S. et al. "QPLL-timed direct-RF sampling band-pass ΔΣ ADC with a 1.2 GHz tuning range in 0.13 µm CMOS." IEEE Radio Frequency Integrated Circuits Symposium, 2011.

[6] Salgado, G.M.; Jovanovic Dolecek, G.; de la Rosa, J.M., "On the use of passive circuits to implement LC-based band-pass CT ΔΣ modulators," IEEE Int. Midwest Symp. Circuits and Systems, pp.1-4, 2015.

[7] D. Akos, M. Stockmaster, J. Tsui, and J. Caschera, "Direct bandpass sampling of multiple distinct RF signals," IEEE Trans. Commun., vol. 47, pp. 983-988, 1999.

[8] Bonacci, David, and Bernard Lacaze. "Lowpass/bandpass signal reconstruction and digital filtering from nonuniform samples." IEEE Int.Conf. on Acoustics, Speech and Signal Process. (ICASSP), 2015.

[9] Azeredo-Leme, C., "Clock Jitter Effects on Sampling: A Tutorial," IEEE Circuits and Systems Maga., vol.11, no.3, pp.26-37, 2011.

[10] B. Mishra, S. Save, and S. Patil, "Design and analysis of second and third order PLL at 450 MHz," *Int. J. VLSI Des. Commun. Syst,* vol. 2, pp. 97-114, 2011.

[11] Ashry, A.; Aboushady, H., "A 4th Order 3.6 GS/s RF ΔΣ ADC With a FoM of 1 pJ/bit," IEEE Trans. Circuits Sys. I, Reg. Papers, vol.60, pp.2606-2617, 2013.