Direct RF Sampling Transceiver Architecture Applied to VHF Radio, ACARS and ELTs

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***Abstract*—Along with the development of aviation industry, there is a rising demand for a breakthrough in avionic systems. The future avionics, besides advancing the current performance and security level, also need to increase the efficiency in size, weight, power and cost (SWaP-C) constraints. Among different solutions, Direct RF Sampling (DRFS) architecture is considered as one of the most promising ones, offering the benefits of hardware simplicity, Integrated Modular Avionic (IMA) and multi-system architecture compatibility. The objective of this paper is to present the new development and implementation of this innovative architecture in both transmission and reception mode. Targeting at some of the most crucial communication systems in VHF avionic bands, including VHF Radio, Aircraft Communication and Address Reporting System (ACARS), and Emergency Locator Transmitter (ELT), this paper describes an approach to create the Signal of Interest (SOI) (transmission) and to process the received signal (reception) in Direct RF, without the LO mixer as in conventional architecture. In addition, in order to demonstrate the advantages of DRFS in future avionics, the paper introduces a solution to improve the coverage and detecting ability of ELT signals. By integrating a spectrum scanner in FPGA, running independently and in parallel with the others avionics, the implementation of this system costs nothing but some FPGA resources, yet reliable and robust. The results show that the DRFS transceiver architecture meets the standards of the regarding avionics (VHF radio, ACARS and ELT). Furthermore, the ELT Detector in FPGA not only can separate the analog ELT signal from other interferences, but also has the sensitivity as good as −100 dBm.**

Keywords—DRFS, ELT, ACARS, VHF Radio, ELT Detector, SDAR

I. INTRODUCTION

The development of RF technology, particularly in Analog/Digital Converters (ADC and DAC) and digital signal processing, has created the opportunities for great breakthroughs in various related domains. Among those, the concentration of aviation is developing the next generation of RF avionics, adapting to the requirements and ambitions of Future Air Navigation System (FANS), and future Communication, Navigation and Surveillance (CNS) avionics.

In recent decades, different efforts have been made to develop new avionic architectures, along with making modifications and suggestions to improve the capacity and performance of the current systems. Since 80s – 90s, a new concept for avionic architecture has been developed, known as IMA architecture. Emphasizing the use of shareable resources to minimize the duplications [1], IMA addresses to a multi-system architecture, in which multiple applications can run independently and in parallel, in one single platform. The concept of IMA has been integrated in the avionics architecture since 2000 [1]. However, due to the limitations of the current RF architectures, these avionic systems cannot be fully integrated, affecting the efficiency in SWaP-C. One of the major problems with these architectures, whether Heterodyne, Superheterodyne or Homodyne, is that only one SOI can be processed in one RF front-end at a time. Therefore, with these architectures, it is impossible to implement a deep-level of hardware sharing components.

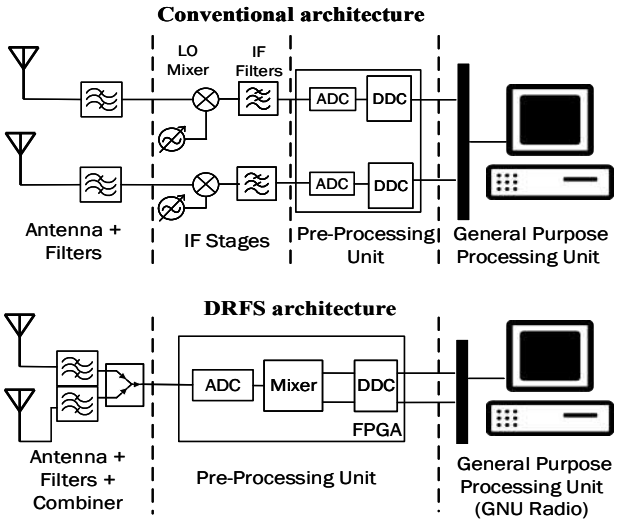

Fig. 1. Conventional vs Direct RF receiver architectures

Recently, with the revolution of high sampling rate ADC/DAC, an alternative architecture, known as Direct RF Sampling (DRFS), appeared and became more and more popular. Based on sub-sampling theory, this architecture offers the possibility to overcome the limitations of its precedent for simultaneous SOI processing. Moreover, since DRFS does not have Intermediate Frequency (IF) stages, it simplifies the RF front-end, hence reduces the effects of the well-known problems in these stages. In other words, DRFS architecture can be considered as one of the promising approaches to meet the requirements of the next avionic generation. Fig. 1 describes the fundamental differences between DRFS and conventional architectures in reception for a two SOI

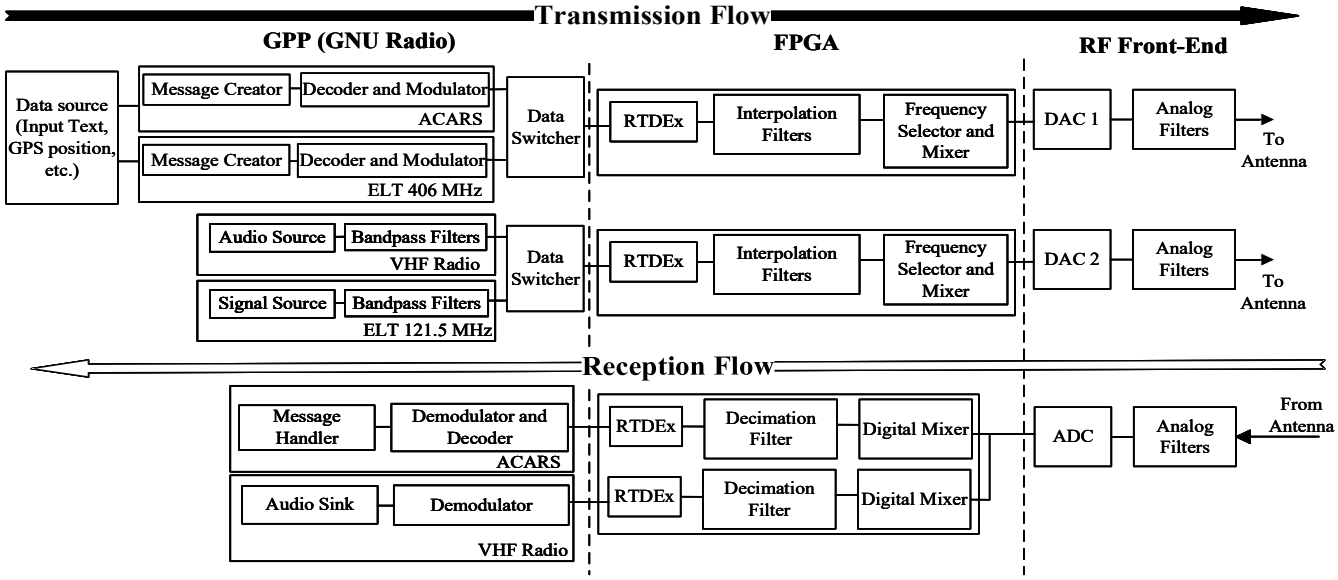

Fig. 2. Block diagram of DRFS transceiver architecture

applications. As it is shown, DRFS replaces the LO Mixer in the conventional architecture with a Digital Mixer after the ADC. By doing so, DRFS gets rid of any components of the IF stages. Furthermore, thanks to folding effect and Digital Mixer [2, 3], multi-SOI in different Nyquist zones can be processed in parallel after the ADC like the conventional system with multiple LO Mixers.

Due to the advantages of Direct RF in avionics, many studies have been done to implement this new technology into real application. One of the first studies of using Direct RF is for Global Navigation Satellite System (GNSS), with the purpose of receiving the messages from multiple transmitters using different carriers. In 1999, Akos et al. [3], using a sampling rate of 15.402 MHz, much lower than the carrier, captured both signals of GPS and GLONASS, proving the capability of using Direct RF, or "direct bandpass sampling" as they called it, in real application. A few years later, Psiaki et al. introduced the experimental implementation of the Direct RF architecture in GNSS, with an important conclusion about the equal performance between this innovative architecture and the conventional superheterodyne [4]. However, due to the limitations of hardware and software at that time, the DRFS architecture did not have the ability to process the GPS signal in real-time, but instead data was stored in a PC and post-test analysis was done to get the final results. Along with the development of technologies, recently, G. Lamontagne [5], introduced the real-time DRFS GNSS receiver. In this study, as summarized in [6], with the sampling rate of hundreds of megahertz, the authors were capable of calculating the reference position, in real-time, with similar accuracy to some state-of-the-art GNSS receivers at that time.

Based on this success, new attempts have been done to implement the DRFS architecture in other aspects of aviation, particularly in RF avionics in navigation, surveillance and communication. In 2015, Yeste-Ojeda and Landry proposed the using of DRFS in VHF avionics, aiming at VHF Omnidirectional Range (VOR), Instrument Landing System (ILS), VHF Radio, ACARS, etc.[7]. Using their approach, the implementation and experimental results of this innovative DRFS architecture were presented in [8] and [9]. As shown in these papers, the sensitivity and dynamic range of the DRFS approach for the target avionics (VOR, ILS) meet the requirements defined by the RTCA [10-12].

This paper focuses on demonstrating the recent integration and implementation of Direct RF for avionics. Because of the nature of the signal, the abovementioned publications focused only on the architecture, the advantages and results in the reception part, even though DRFS architecture can also offer benefits for the transmission part. The work in this article concentrates on communication avionics in VHF band, specifically VHF Radio and ACARS. Furthermore, in order to show the multi-systems adaptability, ELT 121.5 MHz and ELT 406 MHz were developed, integrated and successfully validated by certified equipment. In an emergency, these SOI can be triggered, manually or automatically, and replace the VHF Radio/ACARS transmission channels with high priority signals. Fig. 2 describes this full RX/TX architecture.

Besides, to show the capability of DRFS architecture in future avionics, an ELT 121.5 MHz Detector is developed and integrated in FPGA. Unlike the digital 406.025 MHz, since 2009, this analog distress signal has no more been supported by COSPAS-SARSAT, yet, it is still very popular, particularly among small private airplanes [13]. Using DRFS, a spectrum observer can be integrated in FPGA, using some LUT and Flip-Flop resources. With FFT-based frequency-detecting algorithm, the designed system not only has the ability to separate the real signal from the interferences, but also has a dynamic range from around −10 dBm to approximately −100 dBm. Therefore, the integration of this system in the avionic DRFS architecture will increase the coverage of the distress signal detector network, especially in rural area, reducing the dependency of ELT signal monitor on satellites and ground stations.

In the rest of this paper, Section II briefly describes the important characteristics of the SOI, along with the sub-sampling theory. After that, Section III shows the implementation of VHF Radio/ACARS/ELT in two levels, i.e. FPGA and data generating/processing in General Purpose Processor (GPP). Section IV covers the design and integration of the ELT signal detector, concentrating on the mechanism of separating real distress signal from interferences. In Section V, the performance analysis for all applications (VHF Radio TX/RX, ACARS TX/RX. ELT 121.5/406, ELT Detector) can be found. Finally, the conclusions and perspectives will be presented in Section VI, along with some proposals for further improvement of the performance of the system.

II. THEORIES OVERVIEW

A. Sub-sampling theory in reception and alias utilization in transmission

DRFS architecture, in reception mode, works based on sub-sampling theory, also known as sub-Nyquist sampling theory. Instead of using a sampling rate higher than two times the target frequency, this technique uses a lower rate to convert the analog input into digital values. Taking the advantage of a phenomenon known as folding effect after sampling [2], the target of DRFS is the alias of the SOI falling into the first Nyquist zone. In the same zone, the aliases of any other SOI that have not been attenuated by the Pre-Selection Filters can also be found. In digital domain after the ADC, using Digital Mixer and Decimation Filters, these aliases are separated into channels, moved into baseband and decimated before further processing downstream. The procedure described above can be summarized as in Fig. 3, for an example of two SOI in 2nd and 3rd Nyquist zone. Since the bandwidth of the Nyquist zones is half of the sampling rate, a high speed ADC can offer the 1st zone width enough to cover multiple different SOI. Consequently, multi-system architecture can be achieved, sharing any hardware after the ADC, creating a deep-level integrated RF avionics.

In the transmission (TX), since one DAC can only be used by one application at a time, the level of integration is lower than reception. However, comparing to the conventional architecture, TX in DRFS architecture still has the benefits of being LO Mixer free. In order to bring the signal from baseband to the target SOI, Direct RF uses a combination of interpolation filter and Digital Mixer to create the required output carrier. At the end of this stream, a high sampling rate DAC is used to reconstruct this carrier and creates the required signal. By carefully choosing the sampling rate, type and bandwidth of each filter, and the input frequency, different output carriers can be achieved. Analog filter is integrated at the output of the SDR to eliminate any out-of-interest image. An example of this theory can be found in the next Section, in which the generation of ELT 406.025 MHz is explained.

B. Signal of Interests

In this study, the Signal of Interest are of the communication systems in VHF avionic band, known as ACARS and VHF Radio. These communication avionics require a bidirectional function mode, while digital

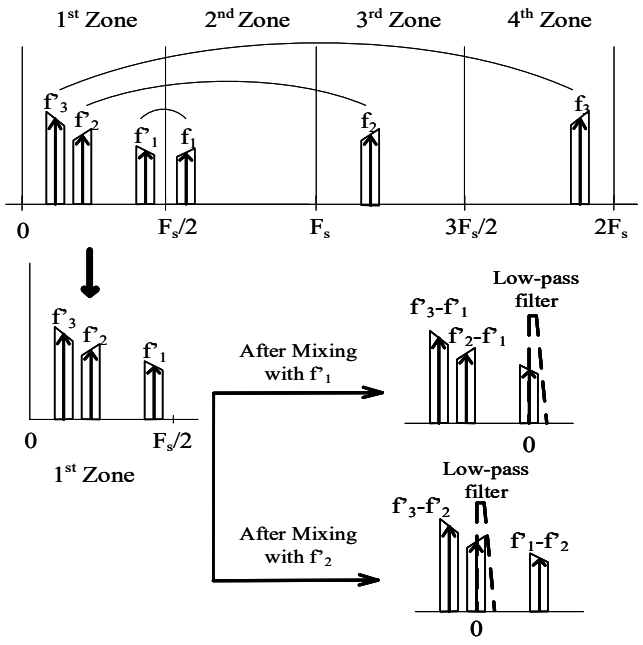

Fig. 3. Fundamentals of DRFS in reception

ELT 406.025 MHz and analog ELT 121.5 MHz are transmission only. Moreover, since distress signals are transmitted only in case of emergencies, in TX mode, two DACs are enough for the integration of four applications. The specific characteristics of each SOI are described below.

ACARS [14]:

- Frequency: 129 MHz – 137 MHz.
- Bandwidth of each channel: ≤ 10 kHz.
- Modulation: Minimum Shift Keying (MSK) with 1200 ± 0.02 % Hz (‘0’) and 2400 ± 0.02 % Hz (‘1’). (The bit ‘0’ represents a bit change from the previous state.).
- Bit rate and sample rate: 2400 bit/s ± 0.02 %; 48000 samples/s.

VHF Radio [15, 16]:

- Frequency: 117.975 – 137.00 MHz.
- Bandwidth: 8.333 kHz, 25 kHz, 50 kHz.
- Modulation type: Amplitude Modulation Double Side Band (AM DSB)
- Audio signal.

ELT 121.5 MHz (i.e. analog ELT) [17]:

- Frequency: 121.5 MHz ± 608 Hz.
- Modulation: AM DSB with modulation factor ≥ 0.85.
- Backward sweep from 1600 Hz to 300 Hz (minimum sweep range of 700 Hz).

ELT 406.025 MHz (i.e. digital ELT) [18]:

- Frequency: 406.025 MHz ± 2 kHz.
- Modulation: Phase Modulation 1.1 ± 0.1 radian peak.
- Message Length: 520 ms ± 1 % (Long Message).
- Message contains ID of the transmitter and GPS position.

Two of the aforementioned applications, ACARS and VHF Radio require both RX and TX, while the ELTs are TX only with higher requirements because of their specific role. The analog distress signal is a continuous audio signal, with a special frequency sweep technique to create a specific emergency audio, whereas the digital signal is a message, containing data.

III. DRFS TRANSCEIVER IMPLEMENTATION

A. General Purpose Processor (GPP)

In the scope of this work, GNU Radio[1] is the backbone of the GPP. Depending on the target avionics, different processing flows are designed in GNU Radio to generate output signals, as well as demodulate, decode and handle input signals. This software-based approach also provides the key for the integration of two applications into one stream, with a switch (manual or automatic) for changing between applications. Fig. 2 shows how the four avionics are integrated in this research. For each of these systems, a more detailed demonstration of their implementation in GNU Radio can be found in the Figs. 4, 5 and 6, corresponding to ACARS, VHF Radio and ELTs (TX).

The basic of the ACARS decoder/demodulator is the FFTW3 library [19], aiming at distinguishing the 2400 Hz and 1200 Hz, which is inspired from the work of Friedt and Goavec-Merou [20]. The calculation is done every 20 samples, using a 1024-point FFT, with a 1004 samples zero-pad. As presented in the diagram at the bottom of Fig. 4, the demodulation/decode process is separated into different levels, from samples (input signal) to message (after confirming CRC).

Fig. 5 and Fig. 6 show the implementation of VHF Radio (TX and RX) and ELT (406.025 MHz and 121.5 MHz), respectively, in GNU Radio. According to the functionality of these avionics, beside the Software Defined Radio (SDR) PicoDigitizer 250, other hardware have to be integrated in the systems, including Audio Sink/Source (Headset) and GPS receiver (u-blox M8T). In order to create the specific sweeping signal for ELT 121.5, a combination of Saw Tooth Source and Voltage Controlled Oscillator (VCO) is used. The relation between sampling rate, frequency, amplitude, and offset of the Saw Tooth determines the output frequencies, repetition period and sweep range of the VCO.

B. FPGA

For reception, as shown in Fig. 1, after ADC, aliases of the target signals in the 1st Nyquist zone are separated into channels using Digital Mixer and Decimation Filters. Fig. 7 shows a closer view of the implementation in this level, for an example with two applications. From 140 Msps, which is the sampling rate of the ADC in this work, the Decimation Filters bring this rate down to 200 ksps, with a bandwidth of 5 kHz for VHF Radio and 10 kHz for ACARS. In order to reduce the order of the Finite Impulse Response (FIR) filters and saving

[1] GNU Radio home site: https://www.gnuradio.org/

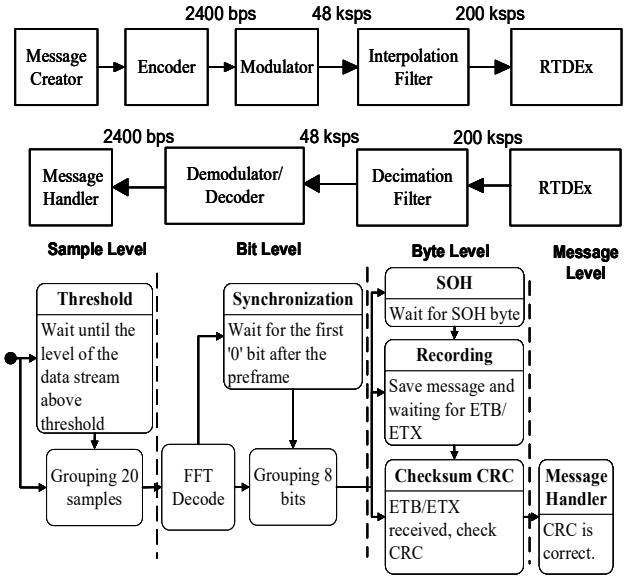

Fig. 4. ACARS implementation in GNU Radio

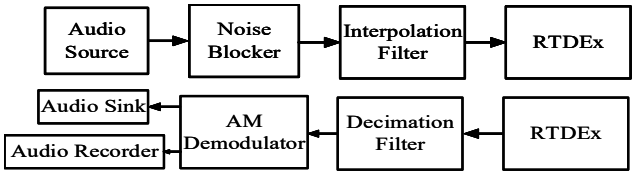

Fig. 5. VHF Radio implementation in GNU Radio

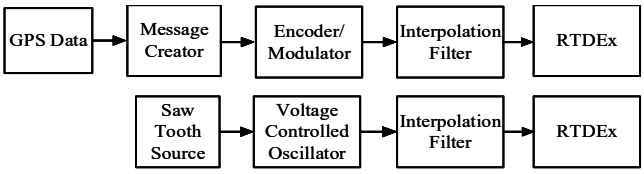

Fig. 6. ELT 121.5/406.025 MHz implementation in GNU Radio

FPGA resources, a cascade between Cascade Integrator-Comb (CIC) and FIR is implemented.

Meanwhile, in transmission, the spectrum utilization of each signal has been already calibrated in GNU Radio for generating process. Therefore, in FPGA, a CIC interpolation filter is enough to up-sample the digital signal. After FPGA level, PicoDigitizer 250 offers two FIR/Coarse Mixer (FIR/CMIX) module running at high sampling rate to interpolate the signal and create the target frequencies before DAC (DAC5682Z, Texas Instrument).

Depending on the reference clock of the FPGA and the selected mode of FIR/CMIX, output signal with carrier up to 1 GHz can be created using a calculated frequency in the Digital Mixer. For example, one of the target signals in this paper is the ELT 406.025 MHz, while the reference clock is the sampling rate of the ADC (140 MHz). Since 406.025 MHz is higher than two times of the sampling rate, it is clear that the two FIR filters need to be set at interpolation mode. A generic

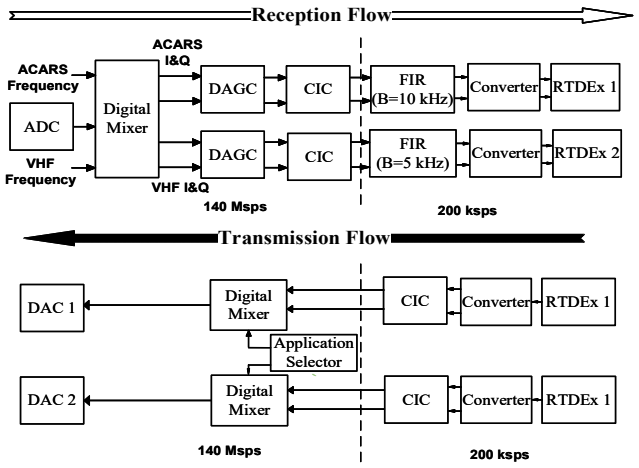

Fig. 7. FPGA implementation for transmission and reception

Input: FPGA sample rate f_s;
Desired signal f;
Number of FIR/CMIX structure N.

Output: Alias frequency f` for Digital Mixer

Initialization

1: Input f;
2: Set $f_{N+1} = f$
LOOP *Process*
3: **for** i = N **downto** 1 **do**
4: $fi = f_{i+1} - N \times f_s$
5: **if** $fi < 0$
6: Set $CMIX_i$ to Low Pass
7: **else**
8: Set $CMIX_i$ to High Pass
9: **endif**
10: $f_i = abs\ (f_i)$
11: **end for**
12: **return** f_1

Fig. 8. Algorithm for calculating the input frequency of the Digital Mixer in DRFS architecture (TX)

algorithm to determine the required input frequency for the Digital Mixer for DRFS architecture is shown in Fig. 8.

IV. FPGA ELT Detector For DRFS Avionic

A. Overview

As mentioned earlier, one of the problems with the analog distress detector network is the limits of coverage and monitor receivers, especially without the supports from the satellites of COSPAS-SARSAT. Due to the limitations of RF avionic architecture, in a real airborne, there is no specific monitoring system for any of the distress frequencies. It can be seen that installing a system that most of the time listen to noise or interference is not a smart solution for aviation, where every extra weight is counted. Nevertheless, analog distress beacon is still popular, especially nowadays when most of the ELT devices are Analog/Digital two-in-one transmitter.

This limit of the conventional architecture, however, is the most important advantage of the DRFS architecture. Benefiting the advantages of folding effect, DRFS architecture can have a system to guard the 121.5 MHz channel, along with any other

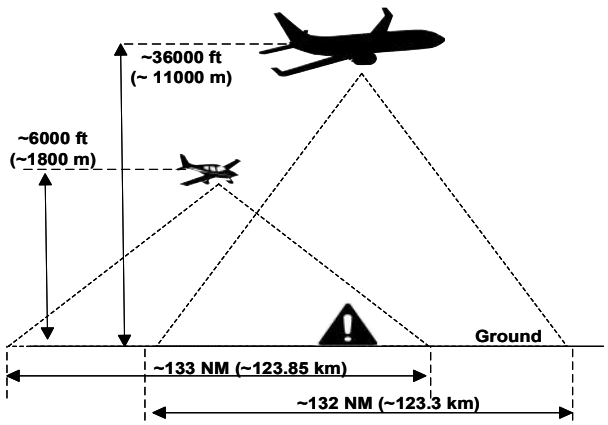

Fig. 9. ELT monitor using integrated system in DRFS architecture

distress frequencies (406 MHz, 243 MHz, 156.025 MHz, etc.) without installing complicated supplementary hardware. Furthermore, by using FFT based spectrum-detecting technique, the proposed ELT detector can separate the real distress signal from the interferences, using just a certain FPGA resources. With this advantage, having an all-time-running robust and sensitive ELT detector in airborne RF avionics is feasible in DRFS architecture. Fig. 9 demonstrates the promising utilization of this ELT detector in aviation. With a sensitivity as low as −100 dBm, which is shown in Section V, the coverage of the developed and integrated ELT monitor is around 65 NM radius regarding the standard transmitted power, calculated by using the simple form of Free-Space Path Loss (FSPL) equation (1) [21]. Even though this coverage is just theoretical, this estimation shows that a worldwide integration of this system in the DRFS architecture is a promising solution to increase the possibility of detecting distress signal in time.

$$FSPL\ (\text{dB}) = 32.45 + 20\times\log_{10}(d_{km}) + 20\times\log_{10}(f_{MHz}) \quad (1)$$

B. Design and Integration

The integration and operation of this detector is in parallel with the main systems, where ACARS, VHF Radio and other systems are being processed. Running at 200 ksps, using 16384-points FFT, the resolution of this system is around 6 Hz for carrier and tones. From the characteristics of analog ELT, the selected parameters, integrated in the developed detector to distinguish the distress signal from others, are:

- The narrow band for the center carrier: 121.4993 MHz to 121.5006 MHz. This value is converted into corresponding FFT bins, eliminating any wrong trigger due to out-of-band interferences.
- The specific frequency sweep of the distress signal, from 1600 Hz down to 300 Hz. The signal with correct carrier but does not have the swept tone in this band will be ignored
- Since most of the ELT transmitters are dual mode, which transmit ELT 121.5/406.025 MHz together, the detection of these two frequencies at the same time will guarantee a real trigger of an ELT device in the area.

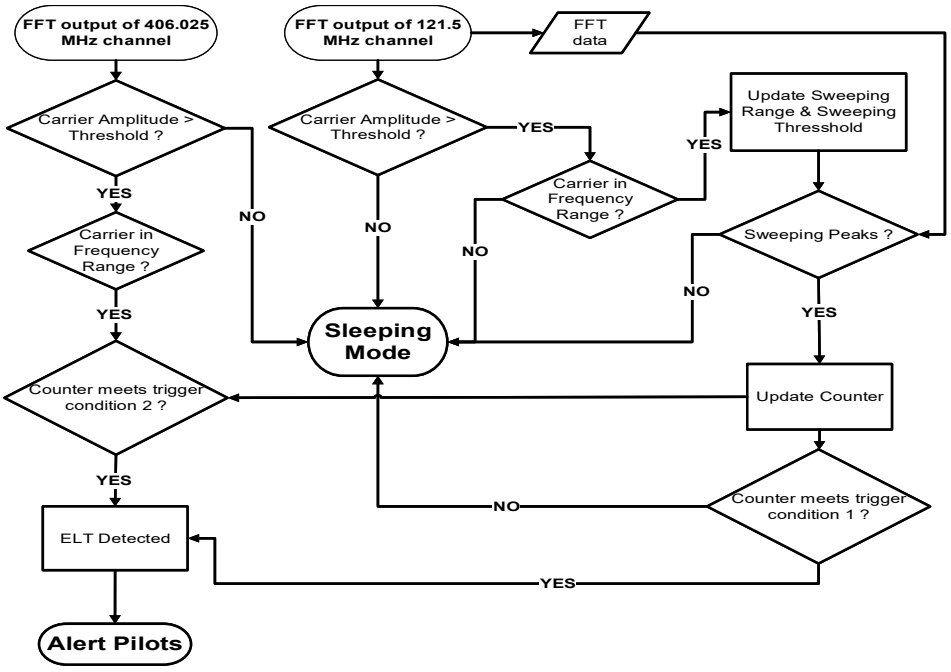

Fig. 10. Flowchart of the ELT Detector in FPGA

Fig. 10 summarizes the developed algorithm for the ELT detectors using FFT bins based on the abovementioned constraints. The combination of different levels of conditions, including the final confirmation and instruction of the pilot in the airplane detecting the ELT signal, will reduce the false trigger rate caused by interferences. In fact, as presented in the next Section, the success and false trigger rate of this system in laboratory tests are almost 100 % and 0 % respectively, with the input level from −10 dBm to −100 dBm. These results are remarkable, regarding the characteristics of the Mid-Range ADC in the developed SDR platform (ADS62P49, Texas Instrument).

V. Performance Analysis

A. VHF Radio: TX and RX

In order to measure the performance of the transmission in the integrated VHF Radio, the SDR platform is configured to transmit a signal with three tones, 350 Hz, 1000 Hz and 2500 Hz, at the same level. The carrier of this signal is at 118.4 MHz, and the gain is set to get the maximum transmitted power. The output of the DAC is connected to an analog filter (100-140 MHz), then wired to a Mixed Domain Oscilloscope (MDO), and Fig. 11 presents the result of this test. At a first glance, it can be seen that the three tones are clearly distinguished from any other frequency, along with the carrier at center. The level of the three tones is still equivalent, even though there is a loss of around 2 dB for 350 Hz, due to the digital filters in both GNU Radio and FPGA. From this figure, with the configuration in the MDO, one can calculate the results in Table I. Using a microphone to have real-time audio signal, the output of this integrated avionic is also verified by Nav/Comm Flightline Test Set (IFR-4000) and other receivers.

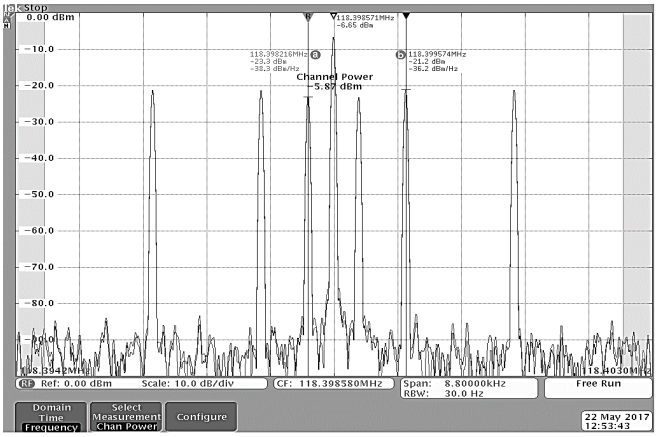

Fig. 11. VHF Radio output with 350 Hz, 1000 Hz, 2500 Hz tones

TABLE I Performance Of The Integrated VHF Radio (TX)

	Standard (Class 4)	**DRFS SDR Performance (without RF Front – End)**
Output Power	4 W (≈36 dBm)	−6 dBm (Max)
Frequency Offset Tolerance	0.003 % (≤ 4kHz)	≤ 0.0015 % (≤ 1500 Hz)
SINAD	6 dB	21.22 dB
Carrier Noise Level vs Signal Level	≥ 35 dB	≥ 70 dB
Channel Selection Time	≤ 1 s	~ 0.5 s
Audio Signal Frequency	350 to 3200 Hz	300 to 3200 Hz

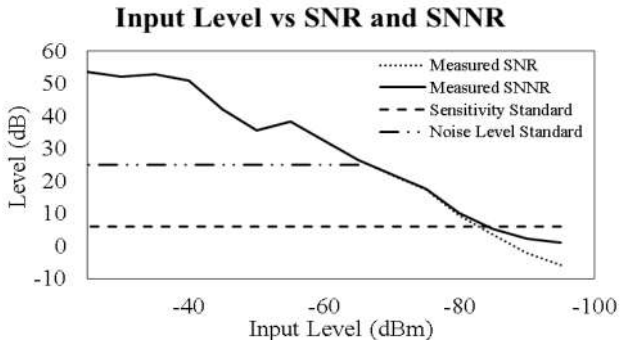

Fig. 12. VHF RX performance

Regarding the standards mentioned in the documents of RTCA [16], in addition to the requirements for output power, this system meets the minimum requirements for an airborne module.

In Reception, using the IFR-4000, we can generate a single tone at 1020 Hz with different levels. Fig. 12 shows the relation between Signal to Noise Ratio (SNR), Signal-plus-Noise to Noise Ratio (SNNR) and input level. Comparing to the standards, this DRFS architecture system meets the requirement for Noise Level, and has the sensitivity of 6 dB lower than the standards.

B. ACARS: TX and RX

The fundamental of ACARS is a specific MSK modulation, with 2400 and 1200 Hz tones. Table II shows the characteristics of the continuous wave 2400 Hz generated at the output of the DAC using DRFS approach, measured by a Vector Signal Analyzer (VSA). This single tone output is equivalent to a series of '1' bits in ACARS signal, as demonstrated previously. In order to compare the performance of the DRFS in transmission mode with conventional architecture using LO Mixer, the results of another SDR platform are also included. This second SDR is calibrated so that the output powers of two SDRs are equivalent.

Even though there are multiple reasons for the differences between the performances of the SDRs, specifically the characteristics of the DAC and the applied architecture, we can acquire some information from Table II. Both of the two architectures have similar results in most of the categories. However, in case of unwanted harmonics, since the DRFS does not use LO Mixer to create the desired carrier, it almost has no problem with the baseband. Any data received by the SDR from the GPP will be transmitted, which means less distortion and a higher level of control. These unwanted side tones might be the reason for the error in demodulation of the VSA in case of the USRP N210 (National Instrument).

In order to verify the correctness of the created message, in particular the parity bits and Cyclic Redundancy Check (CRC),

TABLE II PERFORMANCE OF ACARS IN DRFS ARCHITECTURE (TX)

	DRFS with PicoDigitizer	**Zero-IF with USRP N210**	**Unit**
Output Power	−6.35 (Max Gain)	−6 .29 (Gain 6 dB)	dBm
Carrier Offset	580.97	589.77	Hz
Quadrature Error	0.00 – 0.01	0.00 – 0.06	°
Gain Imbalance	0.00	0.00 – 0.02	dBm
Phase Error	1.00 – 4.00	1.5 – 4.0	°
RHO	0.9999	0.997	
SNR	9.46	10.02	dB
Decode Result	All '1' (Correct)	All '0' (Incorrect)	
Unwanted Harmonics in Baseband	4800 Hz: −70	680 Hz: −48.2 1360 Hz: −55.6 3760 Hz: −62.4 4800 Hz: −60.2	dBc

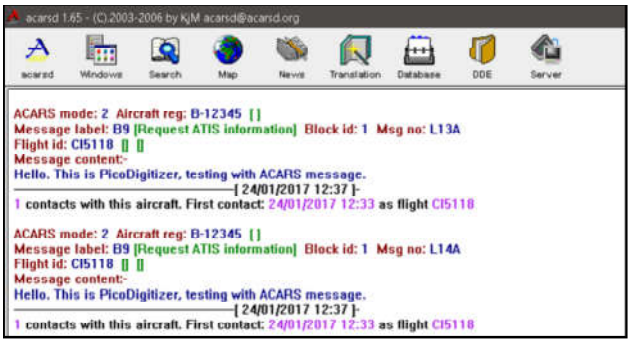

Fig. 13. ACARSD decoded messages

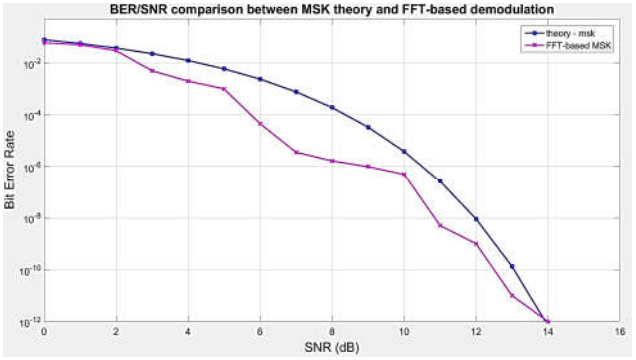

Fig. 14. BER vs SNR for 1024 FFT points MSK demodulator

a third-party freeware, known as ACARSD, has been used to decode the created message. Fig. 13 shows the decoding results in ACARSD for the transmitted message. Since the two flags "Parity Bit", "CRC Check" had been turned on, the displayed results confirmed the CRC, Parity Bit and message format of the created message.

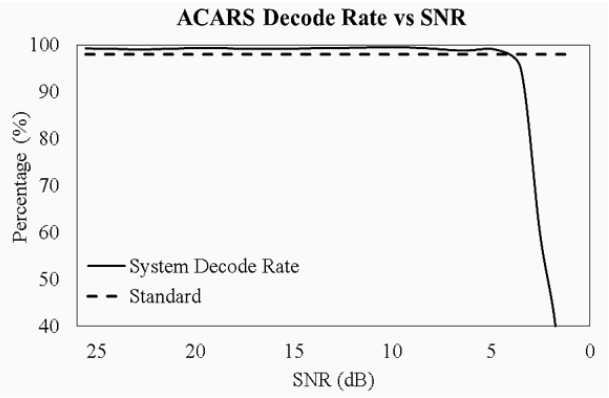

Fig. 15. ACARS Decode Rate vs SNR

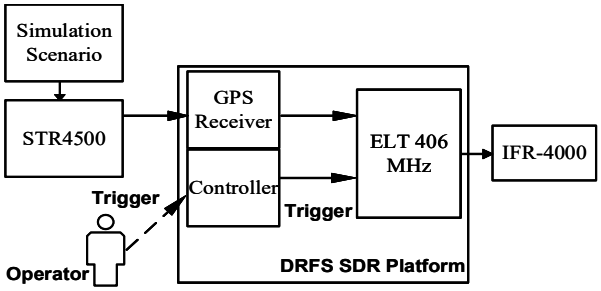

Fig. 16. Test setup for ELT 406 MHz

In reception mode, a test was done to measure the Bit Error Rate (BER) vs SNR of the FFT-based demodulator for ACARS MSK. This BER vs SNR curve is shown in Fig. 14, along with the theory BER/SNR curve of MSK. As can be seen, at the SNR of 12 dB, the BER of the demodulator is below the theoretical value. Therefore, it can be concluded that the integrated ACARS demodulator meets the requirements mentioned in the documents of Aeronautical Radio Incorporated (ARINC) [14]. Fig.15 shows the decode rate of the integrated ACARS as a function of SNR, while the input is a variable message transmitted by a USRP N210. From the receiver characteristics showed in Fig. 12, the maximum and minimum SNR in Fig. 15. are equivalent to the input level between -60 and -85 dBm. Since the requirements for ACARS in reception is a decode rate of 98 % at −100 dBm, a gain around 20 dB is required for this system.

C. ELT 121.5 MHz and ELT 406.025 MHz: Transmission

Table III shows the characteristic of the created ELT 121.5 signal at the output of the PicoDigitizer, measured by IFR-4000 and the MDO. As it can be seen, in addition to the requirements for transmitted power, this system adapted all of the other standards. Since this is the maximum transmitting power of the SDR-in-used, a gain of 30 dB is needed for this system.

IFR-4000 is also used to verify the functionality of the digital ELT. In order to make sure that this system can update the GPS data in real time, a test was done using Spirent Multi-Channel GPS Simulator (STR4500) as the test set up is

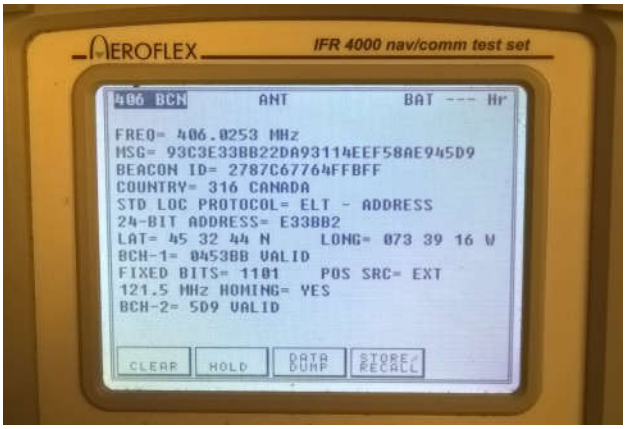

Fig. 17. Result in IFR-4000 of the test for ELT 406 MHz

TABLE III PERFORMANCE OF THE INTEGRATED ELT 121.5

	Standard	**DRFS Performance**
Transmitting Power	20 dBm	−5 dBm (Max)
Center Frequency	121.5 MHz ± 607.5 Hz	121.5000 MHz
Sweep Frequency	1600 – 300 Hz	1444 – 706 Hz
Sweep Range	≥ 700 Hz	734 Hz
Repetition	2-4 Hz	2-3 Hz
Duty Cycle	33% - 55 %	50 %
Modulation Factor	≥ 0.85	≥ 0.99

TABLE IV PERFORMANCE OF THE ELT 406

	Standard (For 144-bit message)	**DRFS Performance**
Transmitting Power	37 dBm ± 2 dB	−5 dBm (Max)
Center Frequency	406.025 MHz ± 2 kHz s	406.0253 MHz
Repetition Period	47.5 – 52.5 second	Normal Distributed within 49 – 51 second
Resolution	4 second	≤ 3 second
Phase Modulated	1.1 ± 0.1	1.1
Transmission Time	520 ms ± 1%	517 ms
Delay from Trigger	≤ 5 minutes	≤ 1 minutes
Correct Format	Confirmed by IFR-4000	

described in Fig. 16. At the beginning of the test, the DRFS system is set at “Normal Mode”, which means ACARS for DAC 1 and VHF Radio for DAC 2. GPS signal generated with a scenario by STR45000 is fed into a GPS receiver (u-blox EVK-M8T). This GPS data is recorded in the GPP by each Coordinated Universal Time (UTC) second. At UTC time equal to 210500, with the reference position N 45°32.7351926’, W 73°39.2697366’, the “Emergency Mode” is activated in DRFS system. The output of DAC 1, which is now ELT 406 MHz, is wired directly to the IFR-4000, and the

output message is shown in Fig. 17. The maximum delay between the trigger and the display is 50 s for 20 tests, including the decoding time in the IFR-4000. From the results in Fig. 17 and Table IV, it can be concluded that the integrated system meets the standards for digital ELT, except the transmitted power, same as all other systems.

D. FPGA ELT Detector using FFT.

In order to measure the performance of the integrated ELT detector, a USRP was used to transmit the analog ELT signal, with its TX port directly wired to the RX port of the PicoDigitizer. The frequency of the carrier and the level of the signal are changed in these tests, from 121.4992 MHz to 121.50075 MHz and -10 dBm to -100 dBm, respectively. The results of the test, which include two hundreds of hours of testing, are summarized in Table V. The average time to detect the presence of real ELT 121.5 signal in the area is less than 30 s, depending on signal level. Furthermore, to make sure that the integrated ELT detector is robust with interferences, the tests were re-done. This time, instead of the correct signal, a constant continuous signal and AM signal without sweeping was used. Since these signals are not the correct distress signal, the ELT detector should not be triggered. For every test, at the end of every hour, the correct ELT signal was transmitted to make sure that the detector is still working properly. So far, no wrong trigger has occurred, neither wrong signal in the distress band (121.5 MHz ± 607.5 Hz) nor correct signal outside of this band. Fig.18 summarizes the probability of correct detecting vs carrier frequency as the results of these tests.

Table VI shows the resource utilization of this implementation in the FPGA platform. As can be seen from this Table, the ELT Detector does not require many resources, except for the RAM/FIFO and slice LUT. These two components are essential for two FFT IP cores as well as logic structures, corresponding to 121.5/406.025 MHz channels.

TABLE V ELT 121.5 DETECTION DELAY

Level	Average Detection Time	Detection Rate
−20 dBm	1.53 s	100 %
−35 dBm	13.82 s	100 %
−65 dBm	20.57 s	100 %
−80 dBm	22.32 s	100 %
−100 dBm	13.62 s	100 %

TABLE VI RESSOURCE UTILIZATION FOR THE ELT DETECTOR (VIRTEX-6VSX315T)

Slice Logic Utilization	In Number	In Percentage
Slice Register	23616	6%
Slice LUTs	15744	8%
Memory	4072	5%
Fully used LUT Flip Flop	2952	6%
RAM/FIFO	205	10%

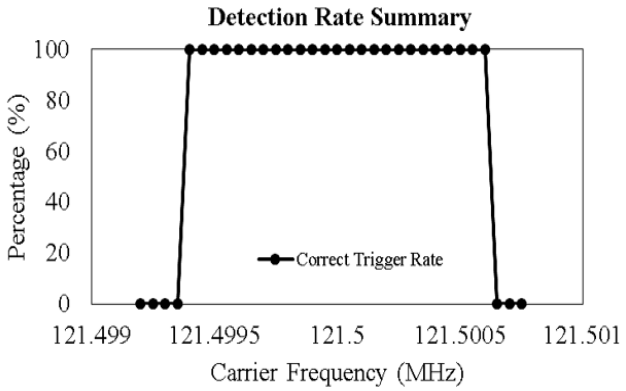

Fig. 18. Detection rate with different carriers

VI. CONCLUSION

In this paper, a DRFS transceiver architecture for VHF avionics has been presented, with detailed explanation about their implementation in different levels, from GPP (GNU Radio) to SDR platform (FPGA). Based on the obtained results, it is clear that the DRFS architecture in combination with SDR can be used for communication avionics, as it is shown for ACARS, VHF radio and Distress Beacon ELT 406.025 MHz and ELT 121.5 MHz. In addition to power transmission, the DRFS transceiver architecture meets the standards of each avionics in certain categories, even though more tests should be performed to validate the functionality of the integrated system, particularly ACARS and VHF radio.

Furthermore, the integration of the ELT Detector, as presented in this paper, shows the advantages of the DRFS comparing to other RF architectures. The results show that the developed module is sensitive and robust while having the ability of separating the correct distress signals from the interferences. Furthermore, the success of the developed module can be expanded to other applications, for example digital ELT and maritime distress signal. If this ELT Detector is integrated worldwide, as a component of the future DRFS avionics, it will surely increase the coverage of distress signal monitoring network. Functioning independent and in parallel with the satellites of COSPAS-SARSAT, the integration of this fully digital module will increase the chance of deploying Search And Rescue mission in time, which increases the safety of aviation. More importantly, the cost of these advantages is only a certain LUT and Flip-Flop components in FPGA.

Although the results show the promising functionality of this turnkey DRFS avionic architecture, there are still many options to improve the system. The same problem of all of the four applications is the transmitting power, which can be overcome by integrating an RF front-end with High Power Amplifier into the architecture. In reception, due to the nature of sub-sampling technique, the RF front-end is also essential, concentrating on the bandpass filters with high out-of-band rejection and configurable Low Noise Amplifier to make sure that the ADC never saturates. For each of the avionics, there are still many different tasks to be done to make sure that a system like this can have the comparable performance with the current-in-use systems. Even though the functionalities of the

FPGA ELT Detector systems have been confirmed, more tests should be performed before having a final validation. Furthermore, along with other avionics, since the laboratory environment cannot have the same characteristics as the real working environment, field tests and later flight tests need to be done to verify the proposed DRFS avionic architecture.

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