Advanced Modeling Technique for Bandpass Continuous-Time Delta-Sigma Modulators

Mohammad Honarparvar[1], René Jr. Landry[1], Frederic Nabki[2] and Mohamad Sawan[3]
[1]LASSENA Research Laboratory, École de Technologie Supérieure,
[2] CoFaMic Research Center, Université du Québec à Montréal,
[3]Polystim Neurotech Lab, Polytechnique Montreal
Montreal, Quebec, Canada
Mohammad.Honarparvar@lassena.etsmtl.ca

***Abstract*—Transistor-level simulations of complex circuits such as delta-sigma modulators (DSMs) that are used to generate highly accurate results are time consuming because of the nonlinear and switched nature of such systems. Therefore, high-level system modeling is required to reduce the simulation time and allow for effective initial design or successive iterations between system-level and transistor-level simulations. Accordingly, a precise behavioral modeling technique for radiofrequency (RF) continuous time (CT) DSM is presented. The main contribution of this work is the differential nature of the RF CT-DSM model in MATLAB such that is it suited for co-simulation in a circuit simulator environment. The modeling technique and simulation methodology are demonstrated toward the implementation of a 4th order RF CT-DSM in MATLAB/SIMULINK environment and a description for each block is provided.**

Keywords-Delta sigma modulator, Continuous-time circuit;Band-pass topology, differential circuits

I. INTRODUCTION

It is a well-established fact that the analog to digital converter (ADC) is the key building block of direct RF sampling receivers and its design is especially challenging at GS/s sampling rates. Nyquist rate ADCs are not well-suited to direct RF receivers because of two main problems: *i*) excessive power consumption and *ii*) low resolution (e.g., ~6 bits for FLASH ADCs). Alternatively, delta sigma modulators (DSMs) are better suited for high dynamic range analog to digital conversion of pass band signals modulated on a carrier frequency. Operational amplifier requirements and settling time constraints limit the application of discrete time (DT) DSMs in GS/s applications. Continuous time (CT) DSMs, on the other hand, take advantage of lower power consumption, higher sampling rate operation as well as provide inherent anti-aliasing filtering. While CT-DSMs can operate at GS/s sampling rates, they suffer from clock jitter, which is the main problem at GS/s sampling rates.

Typically, when designing a CT-DSM, determination of the analog building blocks specifications and optimization of the whole system as well as predicting the behavior of the modulator is time-consuming when using transistor-level simulation. As such, there is a need for faster and accurate simulation methods based on higher-level models for initial design. Although DSM non-ideal modeling was presented in [1] , it is only proposed for low pass DT-DSM. Another behavioral modeling was proposed in [2] for band pass DT-DSMs. In the case of CT-DSM design, behavioral modeling was investigated in [3] for low pass DSMs. In the case of RF CT-DSM, behavioral modeling was presented in Verilog-ATM [4], but has two limitations: *i*) the resonators were implemented using the CT transfer function not through the differential components, and *ii*) the simulation time was increased due to using the combination of Verilog-ATM and SPICE models. Consequently, current modeling techniques cannot present the differential behavior of the transistor-level implementation, and cannot give significant design insight for the circuit-level implementation. Accordingly, high level modeling of RF band pass (BP) CT-DSMs is considered in this paper. The proposed modeling takes advantage of the SimPowerSystems MATLAB toolbox to provide a differential model for RF BP CT-DSM in the SIMULINK environment. Utilizing the MATLAB model in co-simulation with a circuit simulator design environment can be considered as another advantage of this modeling technique. It is to be noted that the current modeling technique can be generalized to other versions of the DSM i.e. active-RC, g_m-C, etc.

This paper is organized as follows: firstly, building blocks of the RF BP CT-DSM are provided in section II. These are followed by the design of a GS/s 4th order BP CT-DSM using the technique. Non-idealities are presented in section III. Simulation results and model evaluation are presented in section IV, and a conclusion is drawn in section V.

II. SIMULINK MODELING OF ANALOG BUILDING BLOCKS

Although, previous work have been focused on usual SIMULINK blocks [1] [2] [3], it is possible to utilize physical components such as resistors, inductors and capacitors within the model [5]. Unlike the previous works, which were implemented in single ended input and output, it is also possible to implement analog building blocks such as g_m-cells in fully differential mode. There are three advantages behind this implementation: *i*) this method provides more accurate depiction of the actual circuit, *ii*) common mode errors can be eliminated, and *iii*) such modeling can be linked to a circuit simulator design environment through MATLAB co-simulation. A link between physical blocks, which are implemented in deferential behavior and usual SIMULINK

978-1-4799-4885-7/14/$31.00 ©2014 IEEE

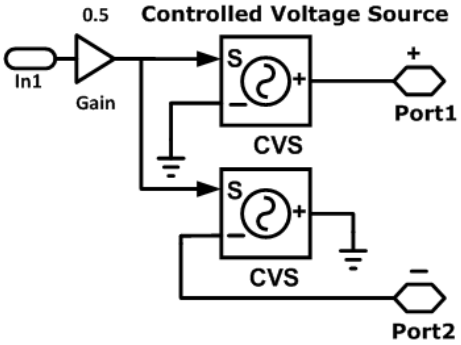


Fig. 1: Single-ended signal-domain to differential physical-domain interface diagram.

model is required as an interface, shown in Fig. 1. To transfer from the signal domain to the physical domain, two controlled voltage sources are required, while the reverse is accomplished via a voltage measurement block.

A. Implementation of the g_m-LC Filter

g_m-*LC* filters are usually preferred to g_m-*C* filters to implement the transfer function of RF CT-DSMs because they can provide a significantly larger dynamic range than g_m-*C* filters. However, g_m-*LC* filters suffer from finite quality (Q) factor, which degrades the performance of the DSM significantly. To enhance the Q-factor, negative resistances can be used. Fig. 2 shows the simplified Q-enhanced filter circuit level and its SIMULINK behavioral model. The implemented transfer function of the filter is given by:

$$H(s)=\frac{\frac{g_m}{C}s}{S^2+\frac{s}{C}\left(\frac{R-R_p}{RR_p}\right)+\omega_\circ^2}\quad,\quad \omega_\circ=\frac{1}{\sqrt{LC}}. \qquad (1)$$

Although any error caused by the g_m-*LC* filter beyond the first stage can be alleviated by the gain of the negative feedback, it should not be ignored for the first stage of the RF CT-DSM. In the g_m-cell of Fig. 2, several non-idealities can be considered such as memory effects, non-linear output current dependence on differential input, and finite output resistance.

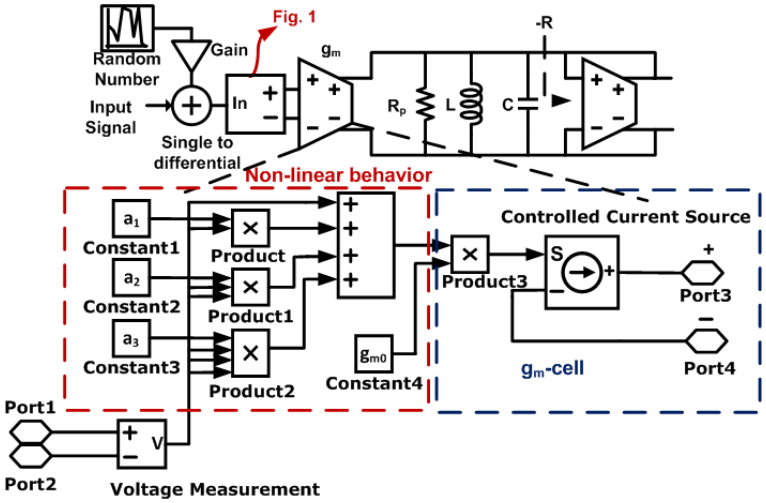


Fig. 2: g_m-*LC* resonator schematic.

These non-idealities can have significant impact on the circuit performance and cannot be underestimated. In general, the non-linear behavior of the transconductance can be expressed as:

$$I=g_{m0}(v_{in}+\alpha_2 v_{in}^2+\alpha_3 v_{in}^3+\ldots), \qquad (2)$$

where g_{m0} is the transconductance and the non-linear coefficients are represented by α_i. It is worth mentioning that the even order harmonics can be considered as zero due to the differential nature of proposed modeling. However, if the even order harmonics are considered, simulation results shows that they do not affect the performance of the modulator. In order to observe how the distortion affects the entire system, the nonlinear behavioral model can be developed in SIMULINK, as depicted in Fig. 2.

Unlike the inner-loop transconductance, any error caused by the input transconductance is injected directly into the loop filter, and degrades the performance of the entire system. This is the case for the intrinsic noise of the transconductance. In this paper, the effect of the intrinsic noise for the input transconductance is investigated. The effect of noise on the input transconductance can be expressed as:

$$V_{out}(t)=V_{in}(t)+V_{noise}.r(t) \qquad (3)$$

where $r(t)$ presents a Gaussian random process with unity standard deviation. This equation can be modeled by a random number block, $n(t)$, followed by gain blocks, V_{noise}, as shown in Fig. 2.

B. Implementation of Quantizer

There are several issues in the implementation of the high speed comparators that are used as quantizer in DSMs: *i*) Metastability of the comparator caused by limited gain of a high speed latch, *ii)* excess loop delay and *iii*) hysteresis effects. Although adding a pre-amplifier stage alleviates the metastability problem, it introduces excess loop delay which may lead to unstable operation. Therefore, the added delay of the quantizer should not be underestimated. Fig. 3 depicts the quantizer model as modeled in [6].

C. Implementation of the DAC

RF CT-DSM design usually begins by the design of the modulator in the DT domain and then mapping the DT-DSM to a CT-DSM using the following transformation:

$$Z^{-1}\{H(z)\}=L^{-1}\{H(s)\cdot H_{DAC}(s)\}\big|_{t=nT_s}. \qquad (4)$$

Therefore, the transfer function of the feedback DAC must be considered in the transformation. The most popular DAC

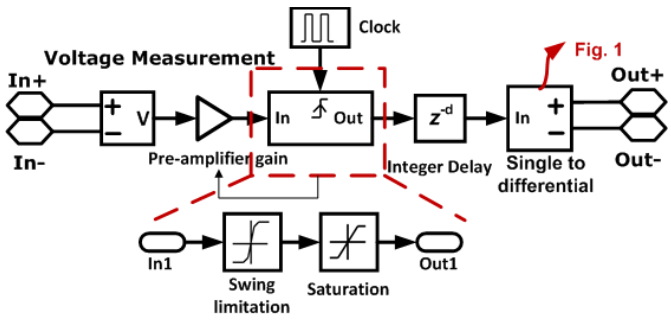


Fig. 3: Quantizer model.

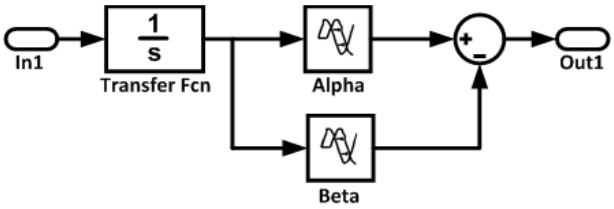


Fig. 4: DAC pulse waveform (α=0, β=T_s for NRZ), (α=0, β=T_s/2 for RZ) and (α= T_s/2, β=T_s for HRZ).

pulse waveforms are non-return-to-zero (NRZ), return-to-zero (RZ) and half-return-to-zero (HRZ). The transfer function of the rectangular DAC waveform can be expressed as:

$$H_{DAC}(S) = \frac{e^{-\alpha s} - e^{-\beta s}}{s}. \qquad (5)$$

It is worth noting that exponential term blocks in Laplace are not defined in the SIMULINK. Therefore, a transport delay block, as illustrated in Fig. 4, can be used to model the exponential term thanks to the following equation:

$$L\{x(t)\,u(t-Ts)\} = X(s)\,e^{-sT_s}. \qquad (6)$$

D. *Effect of Clock Jitter*

CT-DSMs have always suffered from the effect of clock jitter, especially in the case of RF sampling architectures that require very high sample rates. As clock frequency increases, clock jitter becomes a dominant factor in ADC performance. Any momentary variation in the clock period is considered as clock jitter. The main consequence of sampling clock jitter, which whitens the quantization noise, is drastically degrading the performance of the modulator in terms of SNDR. It is worth mentioning that both the quantizer and feedback DAC are exposed to clock jitter effects. However, the sampling error caused by the quantizer can be shaped by the filter, while the sampling error due to the feedback DAC is injected directly into the input of the modulator.

Assuming that the jitter is a Gaussian random process with standard deviation $\delta_i(t)$, the behavior of the modulator can be investigated by the model shown in Fig. 5(a) [1]. However, in the case of modulators with a feed-forward structure and a NRZ feedback waveform, a more efficient method has been

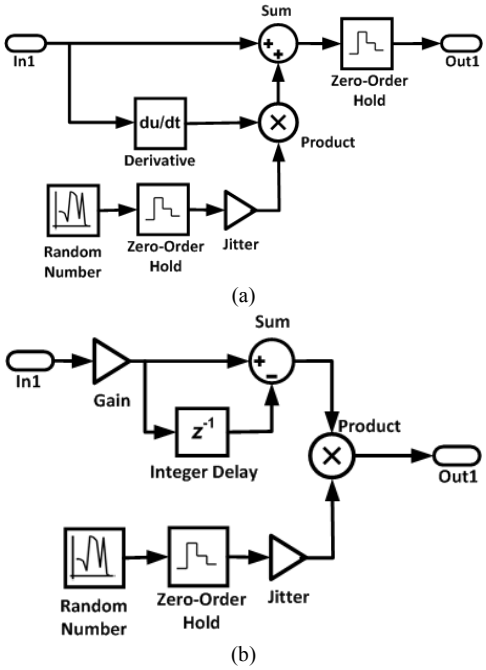


Fig. 5: Jitter model, (a) classical model, and (b) an appropriate model for NRZ feedback DAC.

proposed in [7], and is shown in Fig. 5(b).

E. *Excess Loop Delay*

Excess loop delay (ELD) is another drawback of CT-DSM especially in high speed applications. This effect stems from any delay in the quantizer decision time and DAC output. This delay can make the modulator unstable or can degrade the performance of the modulator by pushing the feedback pulse of one clock cycle into the next cycle. This effect can be modeled by the Transport delay block in SIMULINK.

III. Simulation Results

The design of a 4th order BP CT-DSM with feedback structure [8], shown in Fig. 6, is considered to validate the proposed modeling and apply circuit non-idealities to them. For this design, a 40 GS/s CT-DSM modulator meant to operate with a 2 GHz carrier frequency over a 60 MHz bandwidth is

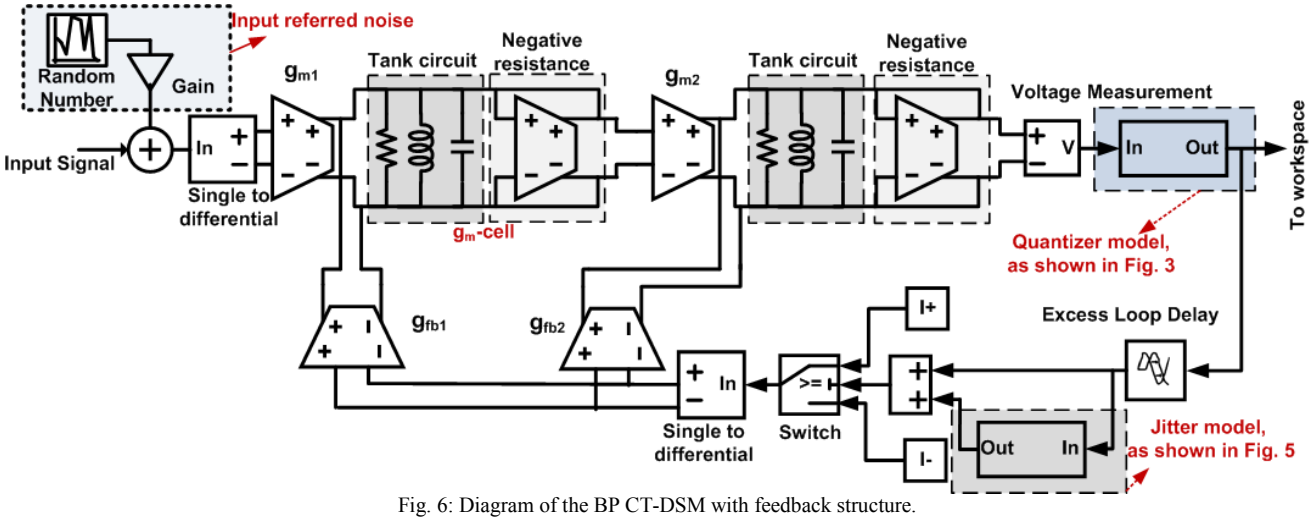


Fig. 6: Diagram of the BP CT-DSM with feedback structure.

considered. Regarding the sampling frequency and bandwidth of the modulator the over sampling ratio (OSR) achieved is of 333.33. The modulator makes use of the feedback structure with only one RZ feedback DAC waveform. Circuit parameters, which are listed in Table I, are extracted from [8] to implement in the SIMULINK environment using the proposed behavioral model.

Fig. 7(a) shows the SNDR of the modulator as a function of loop delay. As can be seen, the modulator shows the maximum SNDR if the loop delay is set to 0.2 times of the sampling period, T_S. However, the modulator must be compensated to become robust against the extra loop delay. Fig. 7(b) shows the SNDR of the modulator versus sampling jitter using the model presented in Fig. 5(a). Time domain simulation result shows that the maximum tolerable clock sampling jitter to avoid more than a 3 dB SNDR degradation is 4% of T_s.

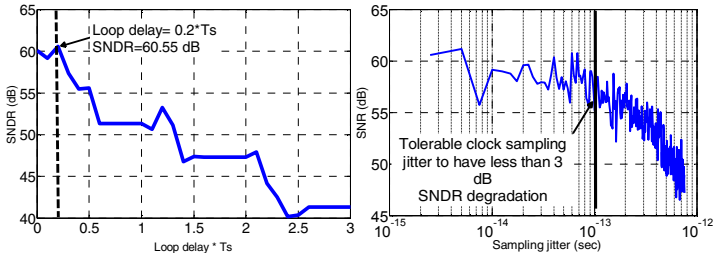
To compare the behavior of the modulator in the presence of non-idealities, the modulator is investigated with the non-idealities listed in Table II and the power spectral density (PSD) and dynamic range (DR) of the modulator are plotted in Fig. 8(a) and Fig. 8(b), respectively. As can be seen from these figures, an SNDR of 60.5 dB can be achieved when the modulator is ideal, while the SNDR degrades to 53 dB, i.e. ENOB of 8.5 bits, in the presence of non-idealities. A comparison between this work and several state of the art modeling techniques is presented in Table III. As can be seen

TABLE I CIRCUIT PARAMETERS OF THE BP CT-DSM DESIGNED IN [8]

Parameter	Value	Parameter	Value
g_{m1}	22 mS	g_{fb1}	50 mS
g_{m2}	10 mS	g_{fb2}	150 mS
L_{tank}	3.8 nH	C_{tank}	2.3 pF

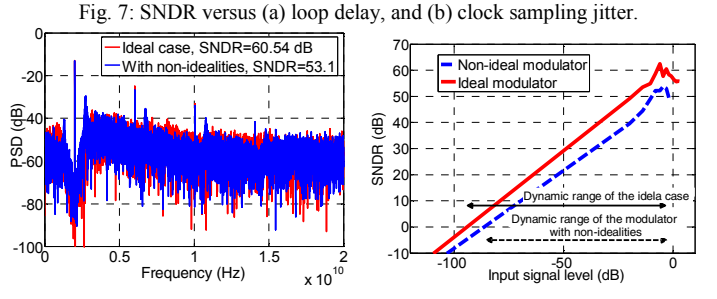
TABLE II MODULATOR NON-IDEALITIES

Parameter	Value
Clock jitter	1%Ts
Excess loop delay	0.5*Ts
Input referred noise	100 μVrms
Linearity	1%



(a) (b)

Fig. 7: SNDR versus (a) loop delay, and (b) clock sampling jitter.



(a) (b)

Fig. 8: (a) Output power spectral density, and (b) dynamic range of the BP CT-DSM.

TABLE III PROPOSED MODELING COMPARISON WITH STATE OF THE ART

Feature	[1]	[2]	[3]	[4]	[9]	This work
Type of Modulator	DT/LP	DT/BP	CT/LP	CT/BP	CT/BP	CT/BP
Verilog-A modeling	N	N	N	Y	Y	N
SIMULINK modeling	Y	Y	Y	N	N	Y
Differential behaviour	N	N	N	N	N	Y
Circuit view modeling	N	N	N	N	N	Y

DT: Discrete Time, CT: Continuous Time, BP: Band Pass, LP: Low Pass, Y: yes, N: no

from this table, the proposed modeling takes the advantage of differential behavior as well as simulation time saving rather than Verilog-A modeling.

IV. CONCLUSION

A fully differential system level modeling for a RF BP CT-DSM has been proposed in this paper. The novelty of the proposed modeling technique lies in the fact that the main building blocks can be implemented in a differential manner which is important from three points of view. First, it gives an intuitive vision from the circuit level. Second, common mode non-ideal effects can be eliminated, and eventually this fully differential modeling is compatible with co-simulation in a circuit simulator environment, especially when full circuit simulation is needed. Ultimately, the presented modeling technique provides a method of investigating the projected circuit-level implementation behavior of the DSM quickly and as a result speed up the design process.

V. ACKNOWLEDGEMENT

This research project entitled “AVIO-505” was supported by the Natural Sciences and Engineering Research Council of Canada (NSERC), the Consortium for Research and Innovation in Aerospace in Quebec (CRIAQ), and with the collaboration of Bombardier Aerospace, MDA and Marinvent. The authors would like to thank the Microsystems Strategic Alliance of Quebec (ReSMiQ) for their support.

REFERENCES

[1] S. Brigati, F. Francesconi, P. Malcovati, D. Tonietto, A. Baschirotto, and F. Maloberti, "Modeling sigma-delta modulator non-idealities in SIMULINK (R)," in *Circuits and Systems, 1999. ISCAS'99. Proceedings of the 1999 IEEE International Symposium on*, 1999, pp. 384-387.

[2] P. Malcovati, S. Brigati, F. Francesconi, F. Maloberti, P. Cusinato, and A. Baschirotto, "Behavioral modeling of switched-capacitor sigma-delta modulators," *Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on*, vol. 50, pp. 352-364, 2003.

[3] P. Aguirre, V. Camargo, H. Klimach, A. Susin, and C. Prior, "Behavioral modeling of continuous-time ΣΔ modulators in matlab/simulink," in *Circuits and Systems (LASCAS), 2013 IEEE Fourth Latin American Symposium on*, 2013, pp. 1-4.

[4] R. Sobot, S. Stapleton, and M. Syrzycki, "Behavioral modeling of continuous time ΔΣ modulators," in *Behavioral Modeling and Simulation, 2003. BMAS 2003. Proceedings of the 2003 International Workshop on*, 2003, pp. 88-91.

[5] Y. H. Leow, F. Zhang, L. L. Teh, and L. Siek, "A circuit based behavioral modeling of Continuous-Time Sigma Delta modulators," in *Integrated Circuits, ISIC'09. Proceedings of the 2009 12th International Symposium on*, 2009, pp. 109-112.

[6] A. Hart and S. P. Voinigescu, "A 1 GHz Bandwidth Low-Pass ΔΣ ADC With 20—50 GHz Adjustable Sampling Rate," *IEEE journal of solid-state circuits*, vol. 44, pp. 1401-1414, 2009.

[7] L. Hernández, A. Wiesbauer, S. Paton, and A. Di Giandomencio, "Modelling and optimization of low pass continuous-time sigma delta modulators for clock jitter noise reduction," in *Circuits and Systems, 2004. ISCAS'04. Proceedings of the 2004 International Symposium on*, 2004, pp. I-1072-5 Vol. 1.

[8] T. Chalvatzis, K. H. Yau, R. A. Aroca, P. Schvan, M.-T. Yang, and S. P. Voinigescu, "Low-voltage topologies for 40-Gb/s circuits in nanoscale CMOS," *Solid-State Circuits, IEEE Journal of*, vol. 42, pp. 1564-1573, 2007.

[9] F. Mannozzi, F. Tinfena, and L. Fanucci, "Sigma delta ADC design using Verilog-A," in *Circuits and Systems, 2003 IEEE 46th Midwest Symposium on*, 2003, pp. 55-58